A study of the charge collection, storage and processing in pixelated semiconductor detectors

DISSERTATION
zur Erlangung des Grades eines Doktors
der Naturwissenschaften

vorgelegt von
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eingereicht bei der Naturwissenschaftlich-Technischen Fakultät
der Universität Siegen
Siegen 2017

Tag der mündlichen Prüfung: 20. März 2017

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Zweitgutachter: Prof. Dr. Ullrich Pietsch

Gedruckt auf alterungsbeständigem holz- und säurefreiem Papier.

Abstract

The new generation of accelerator-based X-ray sources, the so-called free electron lasers (FEL), generate extremely intense, coherent and ultra-brilliant radiation in femtosecond pulses that allow to study nano-structures and ultra-fast processes which were previously inaccessable. In order push the limits of the new radiation sources, detectors are needed that can resolve the enormous contrasts in the experimental data reaching from single photons to 10^5 photons with an energy of 12 keV per pixel per pulse. The pnCCD (pn-junction Charge-Coupled Device) meets the challenges of the new light sources since it can handle high radiation intensities at high readout speeds. However, extremely high photon intensities can result in pixel saturation and charge spilling into neighboring pixels. This charge blooming effect reduces the spatial information for FEL diffraction experiments preventing a reliable image reconstruction.

In this thesis, the collection, storage and processing of signal charges in the pixelated pnCCD semiconductor detector was studied. Experimentally, a laser setup was designed and built to inject different amounts of charges in individual pixels and to scan the pixel structure with high spatial resolution. Numerical device simulations were used to model the electric conditions inside the detector during charge collection, storage and transfer. The simulation results were compared with the experimental data and both were used to establish a physical model for the charge handling capacity of pixelated detectors based on the full depletion of the semiconductor substrate. The results enabled a significant increase of the charge handling capacity and therefore, the dynamic range of the pnCCDs.

Furthermore, it was studied how to remove excess charges from the pixel structure before they spill into neighboring pixels. Since pnCCDs have no closed oxide layer at the register side, there is a direct electric acccess to the semiconductor that allows surplus charges to drain from the device. It was analyzed, if it is possible to establish charge drains in the electric potential of the pnCCD by applying the appropriate operation conditions without modifying the pixel layout or fabrication process. This novel mode of operation opens up a new field in imaging with photons but also with electrons and other charged particles with high intensities.

Zusammenfassung

Die neue Generation beschleunigerbasierter Röntgenquellen, die sogenannten Freien-Elektronen-Laser (FEL), erzeugen ultra-brillante, kohärente Röntgenpulse, welche völlig neue experimentelle Möglichkeiten wie beispielsweise die Untersuchung von Nanostrukturen oder das Auflösen struktureller Details von Reaktionsmechanismen eröffnen. Um die Möglichkeiten, die diese neuen Strahlungsquellen bieten, voll ausnutzen zu können, benötigt man Detektoren, die die enormen Kontraste, die bei FEL-Experimenten auftreten, auflösen können. Bei manchen Experimenten reicht der dynamische Bereich von einzelnen Photonen bis hin zu 10^5 Photonen mit einer Energie von 12 keV pro Pixel und Röntgenpuls. pnCCDs erfüllen die Anforderungen, die diese neuen Röntgenquellen an das Detektorsystem stellen, da sie große Signalladungsmengen mit hoher Geschwindigkeit verarbeiten können. Extrem hohe Photonenintensitäten, können jedoch zu einer Sättigung der Pixel und zum Überlaufen von Signalladung in benachbarte Pixel führen. Aufgrund dieses sogenannten Blooming-Effekts geht ein Teil der räumlichen Information bei Beugungsexperimenten verloren und die Probenstrukturen können nicht mehr zuverlässig rekonstruiert werden.
In dieser Arbeit wird die Sammlung, Speicherung und Verarbeitung von Signalladung in pixelierten Halbleiterdetektoren vom Typ pnCCD untersucht. Für die experimentellen Untersuchungen wurde ein Laseraufbau konstruiert, der es ermöglicht gezielt unterschiedliche Mengen an Signalladungen in die einzelnen Pixel einzubringen und die Pixelstruktur mit hoher Ortsauflösung abzurastern. Mit Hilfe numerischer Bauelementesimulationen wurden die elektrischen Potentialverhältnisse im Detektor während der Ladungsspeicherung, -sammlung und dem -transfer untersucht. Basierend auf den experimentellen Daten und den Simulationsergebnissen wurde ein physikalisches Modell für die Ladungssammlungskapazität volldepletierter, pixelierter Halbleiterdetektoren aufgestellt. Aufgrund der Ergebnisse konnte die Ladungssammlungskapazität und damit der dynamische Bereich der pnCCDs deutlich erhöht werden.
Des Weiteren wurde untersucht, wie sich überschüssige Ladungen aus der Pixelstruktur entfernen lassen, bevor diese in die Nachbarpixel überlaufen. Da pnCCDs keine geschlossene Oxidschicht auf der Registerseite haben, steht ein direkter Zugang zum Halbleiter zur Verfügung, über den überschüssige Ladungen aus dem Bauelement entfernt werden können. Es wird untersucht, ob es möglich ist Ladungssenken im elektrischen Potential der pnCCDs durch Anlegen geeigneter Betriebsspannungen zu erzeugen, ohne die Pixelstruktur oder den Herstellungsprozess zu verändern. Dieser neuartige Betriebsmodus eröffnet ein neues Feld im Bereich der Bildgebung mit Photonen, aber auch mit Elektronen und anderen geladenen Teilchen mit hohen Intensitäten.

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1 Introduction

1.1 pnCCDs in scientific research

Pixelated semiconductor detectors, such as pnCCDs (pn-junction Charge-Coupled Devices), are used in a large variety of scientific applications, like in X-ray astronomy [1] and in experiments at synchrotrons [2] and free electron lasers (FEL) [3]. For those research fields, so-called imaging spectrometers, which are 2D imaging detectors featuring spectroscopic resolution, are required. The pnCCD provides a combination of spatial, spectral and time resolution, which is outstanding compared to other semiconductor detectors. In addition, it is sensitive over a wide energy range reaching from near infrared, over visible light and UV (Ultra Violet), up to X-ray radiation making it the first choice for many experiments.
Originally, pnCCDs were developed as single photon counting X-ray CCDs for astronomical applications at the semiconductor laboratory of the Max Planck Institute for Extraterrestrical Physics (MPE) [4]. Because of their high readout speed, high and homogeneous quantum efficiency, low readout noise and high radiation hardness, they were soon used in a wide range of other scientific disciplines [5].
During the last years, especially imaging experiments in the field of synchrotron research, material sciences and experiments at free electron lasers have benefited from these 2D imaging spectrometers. In particular, free electron lasers offer a variety of new experimental opportunities, but also challenges for the detector system [6], [7]. These accelerator-based light sources, which are currently worldwide under construction, are making a fundamental contribution to the study of dynamic processes at atomic scale. They deliver ultra-brilliant, coherent radiation with 10^{12} - 10^{13} photons per bunch in femtosecond pulses of 10 fs - 100 fs. Thereby, they cover a large range of photon energies from EUV (Extreme Ultra Violet) up to the X-ray regime with very different bandwidths and pulse structures and with micro-bunch repetition rates up to the MHz range.
In the field of biology, this allows to obtain structural information with sub-nanometer resolution of non-crystallizing proteins, viruses or cells before they degrade due to ra-

diation damage [8]. Using pump-probe experiments, it is also possible to film chemical reactions at the atomic scale (figure 1.1). The high brilliance of the FEL X-ray flashes enables scientists to decipher the atomic structure of molecules with only one X-ray flash.
If the sample is brought into the X-ray beam, the photons are scattered and cause a diffraction pattern, which is recorded by the detector system. The atomic structure of the target can then be calculated from the measured intensity distribution by using dedicated algorithms. Depending on the sample, some of the diffraction peaks can be very intense with up to 10^7 X-rays per reflection, while in other areas, only a few photons or no photons hit the detector. Detector systems for FELs must be able to process these extreme differences in the photon intensity. Therefore, the dynamic range of the detector system is crucial for FEL experiments and will be discussed in detail below.

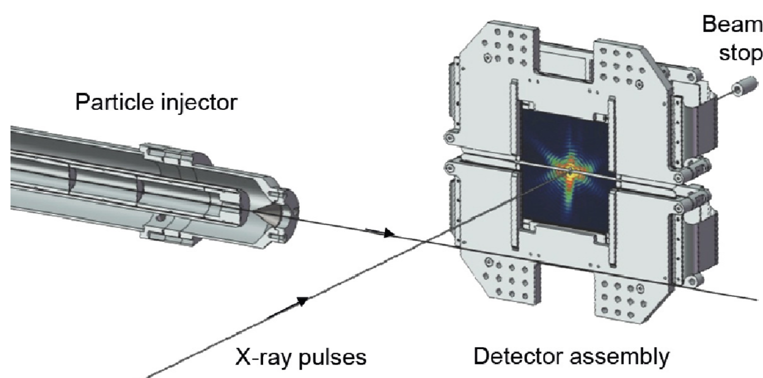

Figure 1.1: Schematic of a diffraction experiment at FEL. The dissolved probe particles, here Mimi virus particles, are injected into the X-ray beam path. The diffraction pattern of each particle, hit by an X-ray pulse, is recorded by the pnCCD detectors. The non-scattered part of the direct beam passes through a hole in the center of the detector assembly before it hits the beam stop [8].

1.2 Dynamic range and charge handling capacity

The ability to properly resolve both very bright and very weak signals in the same image is an essential property of a detector system. The ratio between the largest and the weakest measurable signal is defined as the dynamic range of a detector [9].
When electromagnetic radiation, as for example, visible light or X-rays, impinges on the detector, the photons are converted into signal electrons. Depending on the photon energy, there are different mechanisms for charge carrier generation. The number of generated signal electrons per photon also depends on the photon energy [10]. Conse-

quently, the dynamic range of a CCD detector can be expressed in the maximum and minimum number of electrons that can be measured [11].
The weakest signal that can be detected is not necessarily an electron (which corresponds to a photon in the visible wavelength range [12]). In fact, one has to take into account the minimum electronic noise, which is due to the physical structure of the pnCCD. The amount of signal electrons that would generate the same signal as the noise sigma value is called Equivalent Noise Charge (ENC). In a pnCCD, the ENC is usually between two and four electrons. Thus, the weakest detectable signal is obtained from the readout noise in single photon counting mode. An increase of the dynamic range can therefore be achieved by reducing the readout noise.
However, in experiments with extremely high signals, the maximum detectable signal must be increased. The more photons hit the CCD and the higher their energy is, the more signal electrons are collected in the potential wells of the pixel structure. The maximum amount of charges that can be stored in a potential well and transferred without charge spilling into neighboring wells, is called charge handling capacity (CHC) [11]. The charge handling capacity of pnCCDs with a pixel size of 75 µm × 75 µm under standard operation condition is typically 3×10^5 signal electrons [13]. Once the pixel is saturated, any further charges spill over in the adjacent pixels with the lowest potential barrier for electrons. The total amount of charges is preserved and corresponds to the energy deposited on the detector [14]. Thus, the intensity information is still correct, but the spatial distribution broadens. Since in X-ray diffraction experiments, the structure of the sample is calculated from the position of the reflection peak, the degradation of the spatial intensity distribution results in a loss of the structural information if several peaks overlap [8]. If the exact position of the reflection is lost due to charge spilling into neighboring pixels, the structure can not be calculated (figure 1.2). For this reason, a high charge handling capacity is essential for imaging experiments, especially at free electron lasers, since they emit X-ray flashes with extremely high intensities. However, in some experiments, the reflections are so intense that the signal charges can not be held in a single pixel, even with enhanced pixel full well capacity. This charge spilling causes the so-called blooming effect [11].
In conventional CCDs, different techniques are used to reduce blooming effects [9]. Most CCDs use a vertical antiblooming system, where a reversed-biased junction underneath the pixel is used to drain off excess charges to electrical ground, before they spill over into neighboring pixels. Although the information about the total charge deposited on the detector is lost, the spatial intensity distribution and thus the structural information is preserved.
It has to be taken into account that the maximum detectable signal is not only deter-

mined by the pixel full well capacity. The amount of charges that can be processed, is also affected by the dynamic range of the readout electronics. The detector readout electronics consists of the on-chip electronics, which contains a junction field-effect transistor, and the readout ASIC (Application-Specific Integrated Circuit) named CAMEX (CMOS Analog Mulitplexer) [15]. The amplification of the readout can be adjusted by switchable capacitors, which are part of the amplifier circuit located on the CAMEX chip.

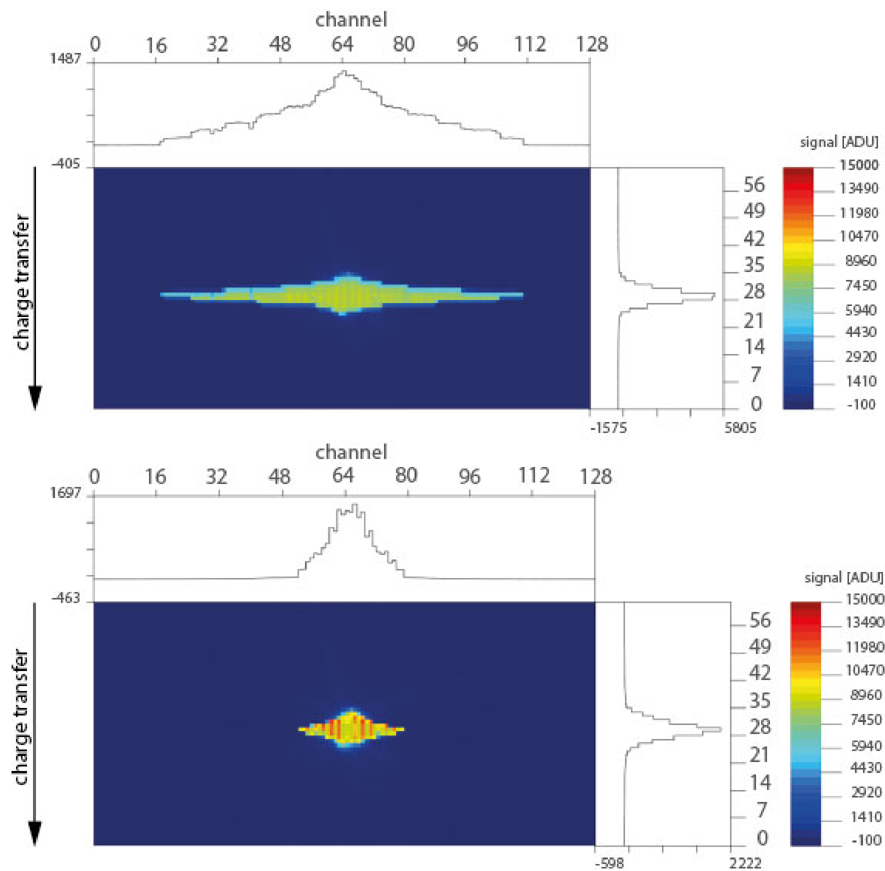

Figure 1.2: Charge distribution for high amounts of signal charges. In both images 1.6×10^8 electrons were generated. In the upper image, the pnCCD was operated in the standard operation mode used for spectroscopy. The charge handling capacity could be increased by a factor of four by changing the operating conditions as done for the lower image [13].

Preliminary experiments showed that by changing the operating parameters of the pnCCD, the charge handling capacity can be improved by a factor of four [13]. Based on these results, it was studied how the dynamic range could be improved even more

to meet the challenges of the new X-ray sources.
The pixel full well capacity was studied experimentally by injecting signal charges with an optical laser and quantifying the charge spilling into neighboring pixels. Numerical device simulations were used to gain a detailed understanding of the electric conditions inside the detector depending on operation parameters and space charge distributions.
With increased charge handling capacity, the number of signal electrons that can be stored in one pixel can no longer be processed with the on-chip electronics. The reason is that the maximum signal is limited by the maximum voltage swing of the readout anode, which corresponds to 8×10^5 signal electrons. The dynamic range of the on-chip electronics was increased by implementing an additional capacitance on the readout anode. So, the maximum possible voltage swing of the on-chip transistor, which is the first amplification stage on the pnCCD, was increased without degrading the linearity of the signal amplitude. Increasing the total capacitance also increases the noise. This can be avoided by increasing the transconductance of the Junction Field-Effect Transistor (JFET) of the on-chip electronics instead.
Furthermore, a mechanism for controlled charge extraction at each pixel will be presented. By adjusting the operation voltages, a direct ohmic contact to the charge content of the pixel is established. This antiblooming mechanism allows draining of charges exceeding a defined drain level, before they spill over into neighboring pixels. The charge drains in the electric potential, which are attractive for electrons, are located under the MOS (Metal-Oxide-Semiconductor) contacts between the channel stop implants. The n-channel MOS contacts are connected to bulk contacts at the sides of the pixel array. The electrons are than drained off to the bulk contacts via the thin conducting charge layer under the MOS contacts. The response of the pixels is linear up to the charge handling capacity in antiblooming mode. The intensity information about the number of surplus charges is lost, but the structural information at diffraction experiments is preserved, even for extremely intense diffraction peaks.

2 Fundamentals of radiation detection

2.1 Basics of semiconductor detector physics

The two basic components of a pnCCD are the pn-junction and the MOS structure. In contrast to insulated gate CCDs, in particular MOSCCDs, the transfer registers of pnCCDs are formed by pn-junctions. This allows for high radiation hardness and fast readout speeds. MOS structures placed between the individual transfer registers form the electric potential of these regions.

2.1.1 pn-junction

A pn-junction is formed by bringing an n-type semiconductor in direct contact with a p-type semiconductor [16], [17]. Due to the concentration gradient of mobile charge carriers, electrons diffuse from the n-type region to the p-type region and leave fixed donor ions with positive charge behind them (figure 2.1). Analogously, holes diffuse to the n-doped region and leave negatively charged acceptor ions behind. The resulting depletion zone is free of charge carriers, except of a small amount of thermally generated electrons and holes. The electric field between these two regions causes a drift current that opposes the diffusion current of the majority charge carriers due to the concentration gradient. In thermal equilibrium, the diffusion current of the majority charge carriers is compensated by the drift current and the net current flow is zero. In this case, the potential gradient, the so-called built-in voltage, is given by [17]:

$$V_{bi} = \frac{kT}{e} ln \left(\frac{N_A N_D}{n_i^2} \right) \tag{2.1}$$

N_A is the acceptor concentration of the p-doped region, N_D the donor concentration of the n-doped region, n_i the intrinsic charge carrier density, e the electron charge, k_B the Boltzman constant and T is the temperature.

The built-in voltage is obtained from the condition that the Fermi levels of the two regions have to line up in thermal equilibrium. The potential difference leads to a

bending of the valence and conduction bands, which can be enhanced or reduced by applying an external voltage V. The voltage across the junction is now $V_{bi} + V$. The pn-junction operates as a diode, allowing an electric current to pass in one direction, while blocking current in the opposite direction. In forward bias, an external voltage $V < 0$ is applied, which means a more negative voltage is applied to the n-contact with respect to the p-contact. In this case, majority carriers are pushed towards the junction from both sides. As a result, the depletion zone reduces and the potential barrier is lowered. As only charge carriers, which are thermally generated inside the depletion region or minority carriers in a distance of a diffusion length around the depletion zone can contribute to the drift current, the diffusion current of the majority charge carriers dominates the net current.
In reverse bias, a voltage $V > 0$ is applied. The majority carriers are pulled away from the junction and the depletion region widens. This increases the potential barrier and reduces the diffusion current of the majority charge carriers. The drift current is still limited by the amount of available minority charge carriers. Therefore, the reverse current increases slowly with the width of the depletion region and the number of the generated charge carriers. The reverse current of a pn-junction is much lower than the forward current and therefore negligible up to electric field intensities where the pn-junction breaks down through avalance and Zener effect.
In a pnCCD, the pn-junction is operated in reverse bias. The width of the depletion region comprises the depletion regions of the n- and p-doped layers. It depends on the doping concentrations and the reverse voltage, which is applied externally [10]:

$$w_d = w_n + w_p = \sqrt{\frac{-2\varepsilon_r \varepsilon_0 \left(V_{bi} + V\right)}{e\left(N_A N_D\right)}} \left[\sqrt{\frac{N_A}{N_D}} + \sqrt{\frac{N_D}{N_A}}\right] \tag{2.2}$$

w_d is the width of the depletion region with ε_0 being the vacuum permittivity and ε_r the relative static permittivity of the semiconductor. N_A is the acceptor concentration in the p-doped region, N_D the donor concentration in the n-doped region, e the electron charge, V_{bi} the built-in voltage and V the external voltage.
With appropriate low dopant concentrations, large regions of the pn-junction can be depleted. In the asymmetric case $N_A << N_D$, the width w_n is much larger than w_p. In the pnCCD, p-contacts with a high dopant concentration are implanted on a weakly n-doped substrate to deplete the full width of the substrate.
In semiconductor radiation detectors, the depletion layer serves as the sensitive volume for incident X-rays. The absorption of photons leads to the generation of electron-hole pairs, which are separated in the depletion region. The electrons and holes drift

in opposite directions. This transport process generates an electric current, which corresponds to the absorbed energy.

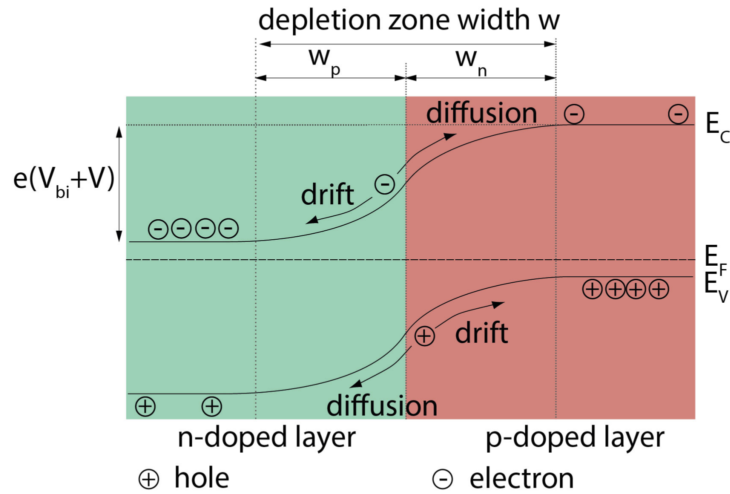

Figure 2.1: Abrupt pn-junction in thermal equilibrium. In thermal equilibrium, drift and the majority charge carrier diffusion current lead to the depletion of the transition region. The electric field in the depletion region is caused by the remaining donor and acceptor ions. This results in a potential barrier V_{bi}, which can be increased or decreased by an external voltage V.

2.1.2 MOS structure

A MOS capacitor consists of a semiconductor (here silicon with a bandgap of 1.12 eV), an insulator (here silicon oxide with a bandgap of 9 eV) and a metal layer (here aluminium). In a pnCCD, the p-implanted registers at the front side are separated by MOS contacts. By applying a gate voltage, an electric field is generated on the surface of the silicon, which is proportional to the induced surface charge. The electric field is shielded in the interior of the silicon by the induced space charge layer, which is caused by reassignment of impurities and changed in the density of mobile charge carriers. Ψ_B represents the Fermi potential with respect to the intrinsic energy E_i (figure 2.2). The electric potential, which is determined by the gate voltage, leads to a band bending Ψ_S in the space charge layer. The potential distribution can be calculated using the Poisson's equation of electrostatics. The boundary conditions are the absence of the electric field inside the semiconductor and that the electric field at the surface has to be proportional to the induced surface charge. The space charge density depends on the energy difference between the conduction band E_C and the Fermi level E_F, as well as on the difference between the valence band E_V and the Fermi level. The exact mathe-

matical description is given in [17].
For an n-doped substrate, the four different operation modes (figure 2.2), depending on the applied gate voltage V, are:

- **A) Flatband condition**: The charge carrier concentration in the homogeneously doped n-type silicon is the same as at the interface of the oxide. The electric field inside the semiconductor is zero. For the flatband voltage V_{FB}, there is no charge on the plates of the capacitor and hence there is no electric field across the oxide.

- **B) Accumulation**: A positive gate voltage larger than the flatband voltage induces positive charges on the metal contact and negative charges in the semiconductor. The electrons accumulate at the silicon-oxide interface and the energy bands in the semiconductor will bend downwards.

- **C) Depletion**: If a voltage that is more negative than the flatband voltage is applied to the gate, the electrons are pushed away from the gate and inside the semiconductor. The density of free electrons becomes negligible compared to the rest of the semiconductor. The boundary zone is depleted from mobile charge carriers and the energy bands are bent upwards. In MOSCCDs, the depletion region is the sensitive detector volume.

- **D) Inversion**: If the gate voltage is further decreased, the intrinsic level at the semiconductor-oxide interface will reach or even cross the Fermi level. Therefore, the minority charge carrier density exceeds the majority charge carrier density at the interface. This condition is called weak inversion. If the gate voltage is further decreased, a p-channel is generated at the inside of the semiconductor at the interface to the insulator and p-type conductivity is possible. The charge of the holes in the p-channel decreases the vertical space charge region compared to depletion.

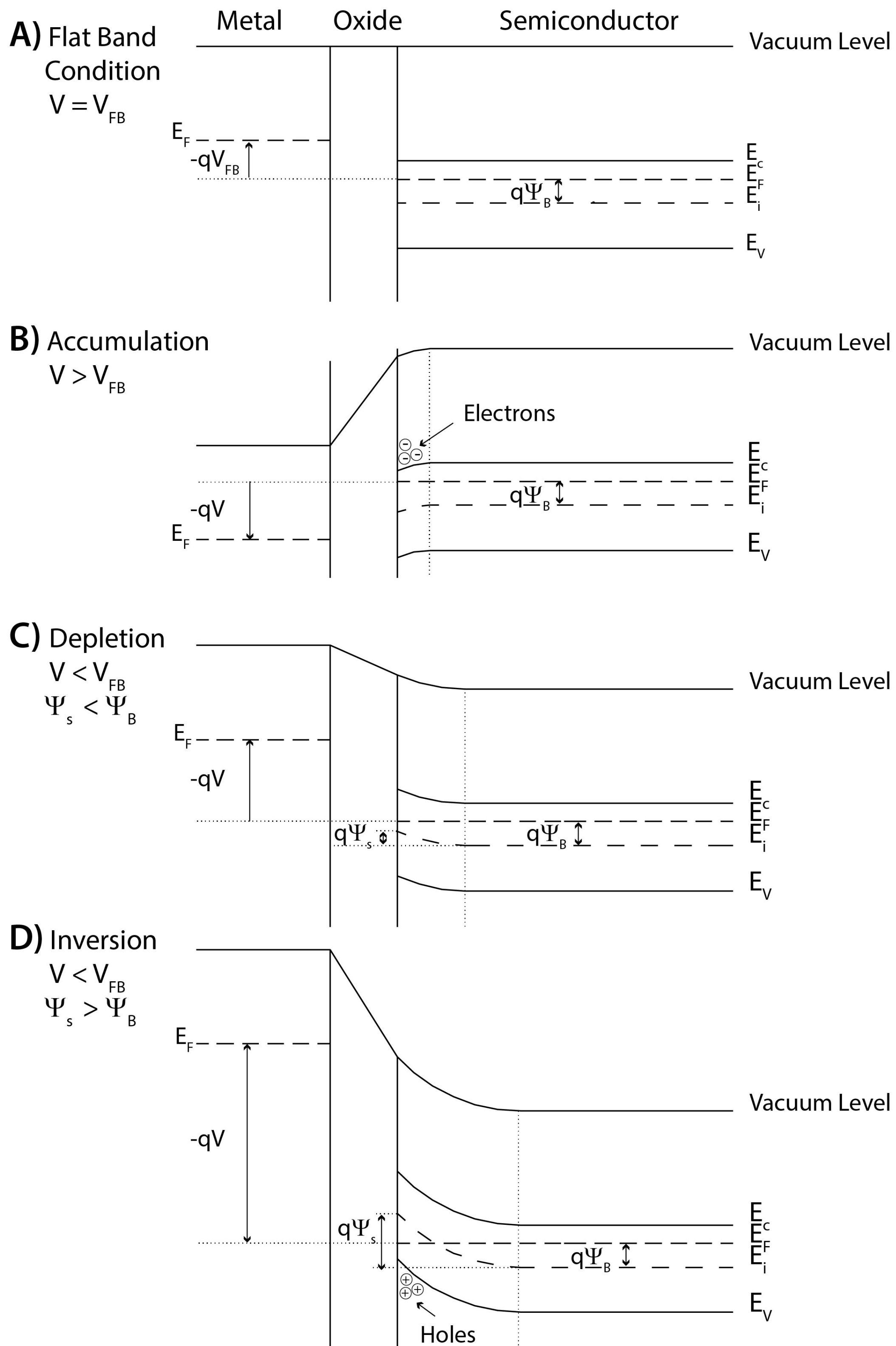

Figure 2.2: Schematic of a MOS capacitor on n-doped silicon. Under flat-band condition the electric field is zero (A). In accumulation (B), the electron density at the silicon-oxide interface is much higher than in the bulk. If the MOS structure is depleted (C), the electron density is negligible compared to the bulk up to the depletion depth. In inversion (D), the vertical space charge region is decreased compared to depletion.

2.2 Interaction of electromagnetic radiation with matter

pnCCDs are mainly used for radiation detection in the energy range from 30 eV to 30 keV. In this energy range, the interaction of photons with silicon is dominated by the photoelectric effect [16], [10]. This means, that the photon is absorbed by an atom and transfers its energy to the emitted electron.

In a semiconductor, the photon excites an electron over the band gap and the remaining energy is transformed into the kinetic energy of the electron. The band gap of the semiconductor material defines the minimum required energy to generate an electron-hole pair. For silicon, the minimum energy at room temperature is 1.12 eV. This corresponds to an optical photon with a maximum wavelength of 1100 nm. For higher photon energies, the excited electron loses its energy mainly by generating either phonons or electron-hole pairs via Coulomb interaction with other electrons from the valence band. Since a part of the photon energy is transfered to the crystal lattice, the average energy that is required to generate an electron-hole pair in silicon is 3.65 eV. Although deviations occur for photon energies close to the band gap energy, this value is considered to be constant.

The statistical fluctuation of the average number of electron-hole pairs that are generated, is given by the so-called Fano noise [10]. The Fano noise intrinsically limits the energy resolution of the detector. The electron leaves the atomic shell with the energy E - B. E is the energy of the primary photon and B is the binding energy of the electron. While subsequent ionization processes occur, the electron generates secondary charge carriers. The excited atom releases to the ground state by emitting energy in form of fluorescence radiation and phonons. Normally, the emitted fluorescence photon interacts with other atoms of the semiconductor or it transfers its energy directly to the electrons of the radiating atom. This process is called the Auger effect and leads to Auger electrons with a short range. In both cases, the secondary interaction leads to a detectable signal. The energy of the incident photon is completely deposited in the volume of the detector. If the fluorescence photon leaves the detector without any further interactions, the incident photon will be detected with a reduced energy, giving rise to the so-called escape peak.

In this work, the processing of high amounts of signal charges was investigated with an optical laser setup. The interaction of optical photons with matter differs from that of X-ray photons. X-ray photons are much more energetic and can reach the inner shells of atoms and ionize them with only one single photon. Optical photons interact with the outer valence electrons. For the following considerations, only the amount of signal electrons reaching the register side is important and not their generation process.

At high intensities, the electron-hole pairs create a so-called electron-hole plasma, which influences the electric field inside the detector. The boundary of the plasma cloud is an equipotential area and the charges of the interior of the charge cloud are shielded from the outer electric field. Only the charge carriers at the outer boundary of the charge cloud are influenced by the electric field and they begin to migrate promptly. The charge carriers of the outer region of the plasma cloud are removed until the charges of the interior are exposed to the electric field and also begin to drift. This effect can be neglected at low charge carrier densities, whereas if the charge carrier density exceeds the bulk doping of the detector, the changes in the electric field dominate the charge collection process. This results in an increase of the charge collection time (figure 2.3) and the spatial distribution of the charge cloud (figure 2.4) [18]. Self-shielding effects inside the plasma lead to field free regions and ambipolar diffusion becomes the dominant charge transport process.

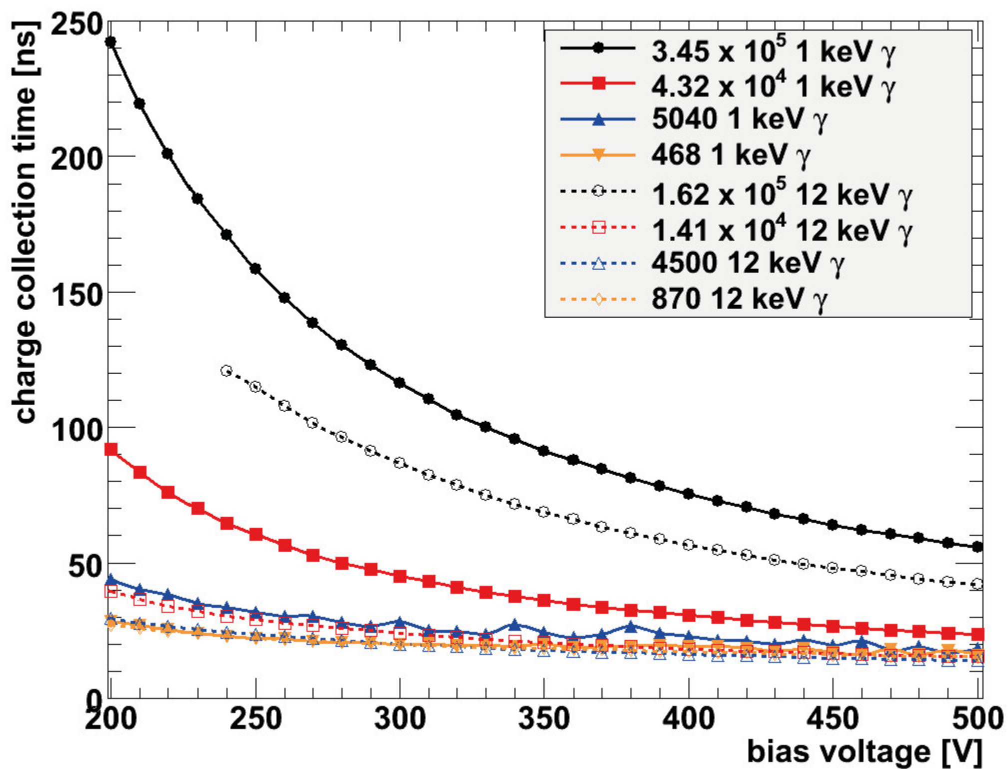

Figure 2.3: Charge collection time as function of the bias voltage. The curves show the charge collection time of a 450 μm thick silicon detector as a function of the applied bias voltage for different laser intensities of 660 nm (1 keV γ) and 1015 nm (12 keV γ) wavelength [18].

Since the plasma dissolves slowly, it increases the charge collection time by the so-called plasma delay. The plasma delay is the time required for the charge cloud to disperse to the point where normal charge collection begins. During the charge collection time the charge carriers drift apart laterally due to diffusion and electrostatic repulsion. Electrostatic repulsion and diffusion decreases the charge carrier density and the lateral spread of the collected charge. It has been shown that the lateral spread is a strong function of the electric field inside the detector and therefore the bias voltage. So, high bias voltages counteract the plasma effects as the self-shielding effects of high charge carrier densities are reduced. In order to reduce the effects of the expanding plasma at high charge carrier densities, an integration time that exceeds the maximum charge collection time with the plasma delay and a pixel size larger than the charge spread determined in [18] were chosen for the following study.

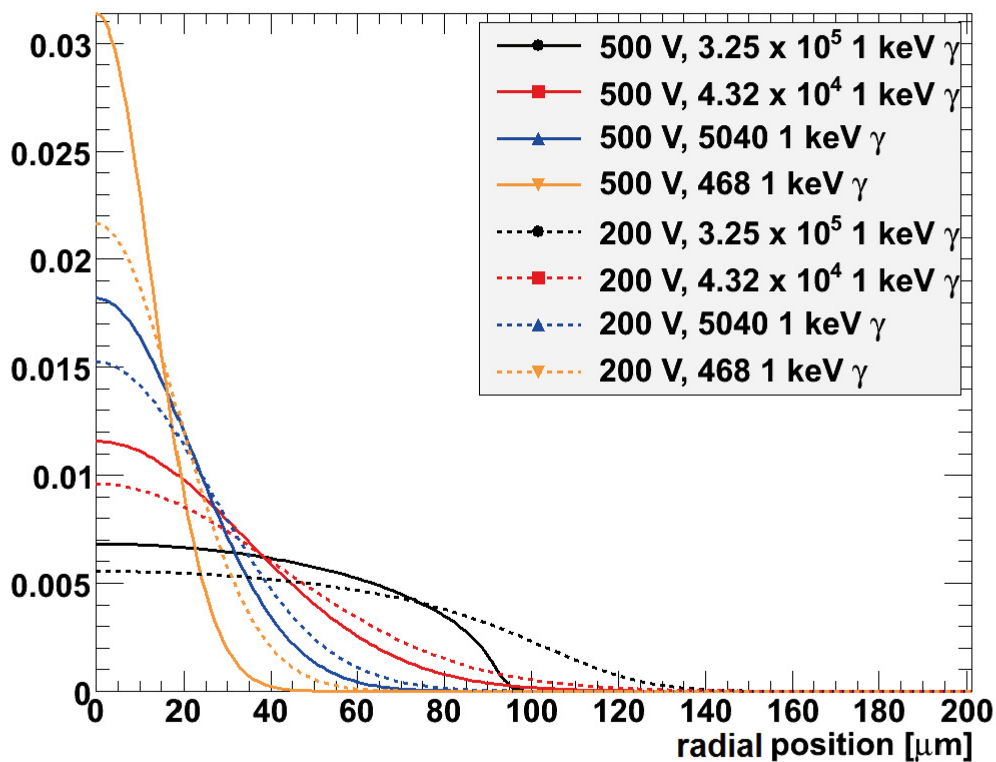

Figure 2.4: Radial point spread function of a 450 μm thick silicon detector. The curves show fit results for 200 V (dashed lines) and 500 V (solid lines) bias voltage. The sigma of the laser light is approximately 3 μm and the wavelength is 660 nm [18].

3 The pnCCD detector

3.1 pnCCD principle

In pnCCDs, the energy of the detected photon is resolved by the amount of charges created in the silicon bulk. In order to obtain a very precise quantitative detection of the amount of signal charges generated by the incoming photons, the detector has to be depleted of other mobile charge carriers as they provide a noise contribution. pnCCDs are based on the principle of sidewards depletion proposed by Gatti and Rehak [19] in 1984. The concept of sideward depletion is that a large, weakly n-doped (n^-) silicon wafer can be fully depleted by a small heavily n-doped (n^+) ohmic contact, which is positively biased with respect to the p^+-contacts covering both surfaces of the silicon bulk. So, the full pnCCD thickness of 450 µm can be depleted by a strongly doped n^+-contact serving as readout anode, by using a reverse biased pnp-structure. With increasing reverse voltage, the depletion regions from the p^+-implants, which are the back contact and the shift registers, are extending into the bulk until they join, so that the whole volume is depleted.
Since the device is depleted from both sides, only a quarter of the voltage required to fully deplete a diode of the same thickness is needed (equation (2.2)). In the middle of the bulk, where the two depletion zones meet, the electric potential has a minimum for electrons. By applying a more negative voltage difference between the back contact and front side than the depletion voltage, the potential minimum is shifted closer to the side containing the pixel structure, which is denoted as front side. In standard operation mode used for spectroscopy, the potential minimum und thus the storage depth of the electrons is at a depth of 7 µm below the front side (figure 3.1).

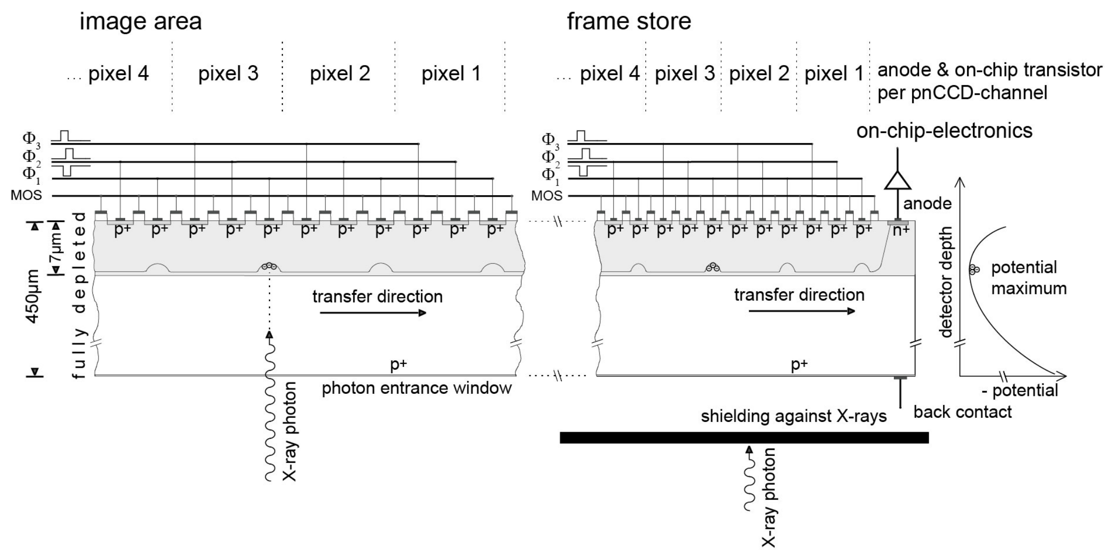

Figure 3.1: Principle of the pnCCD. The silicon bulk is fully depleted mainly due to the negative back contact voltage. The signal electrons are stored in the potential minima under the p^+-registers. After reaching the last register, the electrons drift to the readout anode. The readout anode has a more positive potential than the registers and therefore forms a local potential minimum for electrons. The signal electrons cause a voltage swing on the readout anode, which is connected to the gate of the on-chip transistor.

A high-energy phosphorous implantation (HE-implantation) additionally defines the transfer channel in this depth. Photons that hit the pnCCD at the entrance window at the back side, generate electron-hole pairs in the bulk. Because of the applied voltages, a potential gradient is generated and the holes drift to the p^+-implanted back side, whereas the electrons accumlate below the register side. The graph on the right hand side of figure 3.1 shows a schematic of the potential gradient in the pnCCD bulk. The potential maximum, which is the minimum for electrons, is at a depth of 7 µm below the front side.

In addition to the pn-structure across the bulk, the pixel structure at the front side of the device also consists of pn-junctions. The contact at the front side is structured into p^+-doped stripes forming the so-called p^+-shift registers (figure 3.1). By applying external voltages to the p^+-transfer registers, local potential minima for signal electrons are formed. A pixel consists of three p^+-registers with the electric potentials Φ_1, Φ_2 and Φ_3. Therefore, the respective transfer registers are also denoted with Φ_1, Φ_2 and Φ_3.

In row direction, which is perpendicular to the transfer direction, the pixels are separated by electric space charge regions, the so-called channel stops, which are formed by p-implants. The charges are shifted to the readout by a three-phase transfer, where every third register electrode has the same potential (figure 3.2).

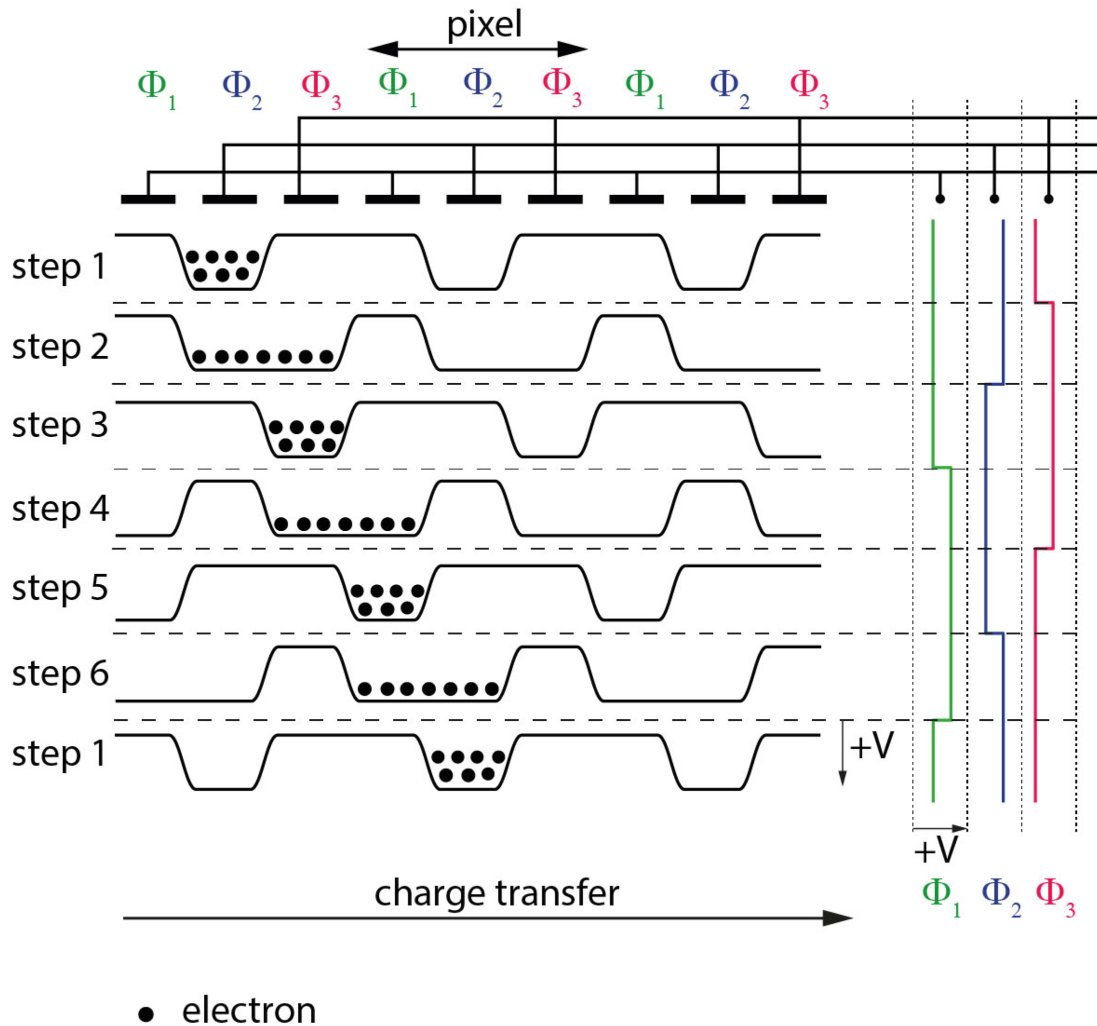

Figure 3.2: Clocking scheme of a three-phase pnCCD. The electrons are stored under the register with the more positive voltage. Here, the signal charges are initially stored under Φ_2. The transfer of the signal electrons to the readout is done by sequentially switching the register voltages between a positive and a negative value. On the right side, the timing diagram used to transfer the electrons to the right, is shown.

By periodically altering the register voltages, the charges are transferred along the channels. At the end of each channel, the charge packages are shifted to the readout

anode. The anode is connected to the gate of a JFET (Junction Field-Effect Transistor), the so-called first FET, integrated in the pnCCD structure, which serves as first readout amplifier.
The efficiency of the charge shift is determined by the so-called charge transfer efficiency (CTE). The CTE gives the relative amount of signal charges which are shifted from one pixel to another:

$$CTE = \frac{Q_{n+1}}{Q_n} \tag{3.1}$$

where Q_{n+1} and Q_n are the number of charges located in pixel $n+1$ respectively n, when the signal charges were transfered from pixel $n+1$ to pixel n. Its complement, the charge transfer inefficiency (CTI), is defined as

$$CTI = 1 - CTE \tag{3.2}$$

It gives the relative amount of charge loss after one pixel transfer. Charge transfer losses occur due to defects in the silicon crystal, which provide energy states in the silicon band gap. Signal electrons can be trapped by the defect energy states located in the region of the transfer channel. The mean number of signal electrons which are trapped during the transfer from one pixel to the next determines the charge transfer loss. In pnCCDs, the CTI is typically as low as 10^{-5}.

3.2 pnCCD structure

3.2.1 Pixel array

The pixel matrix of a pnCCD is formed by repeating the structure of a pixel in the row direction and the channel direction, which is the charge transfer direction. The pnCCDs used in this study have a pixel size of either 75 µm × 75 µm or 48 µm × 48 µm. Each pixel is composed of a set of ion implantations, insulator layers and aluminium contacts (figure 3.3).
The shift registers are realized by long strip-like p^+-implants extending across the whole width of the device. The electric contact is established via an aluminium layer, which has approximately half the width of the p^+-implant. The electric potential between the p^+-registers is defined by MOS structures, consisting of an aluminium and oxide layer on top of the silicon substrate. The channel structure of the pnCCD is defined by deep

n- and p-implants, located below the p^+-registers. In the row direction, deep n-implants the so-called channel guides, define the pixel border (figure 3.3). Deep p-type implants, placed between the n-channel guides, the so-called channel stops, serve as additional potential barriers and separate the transfer channels.

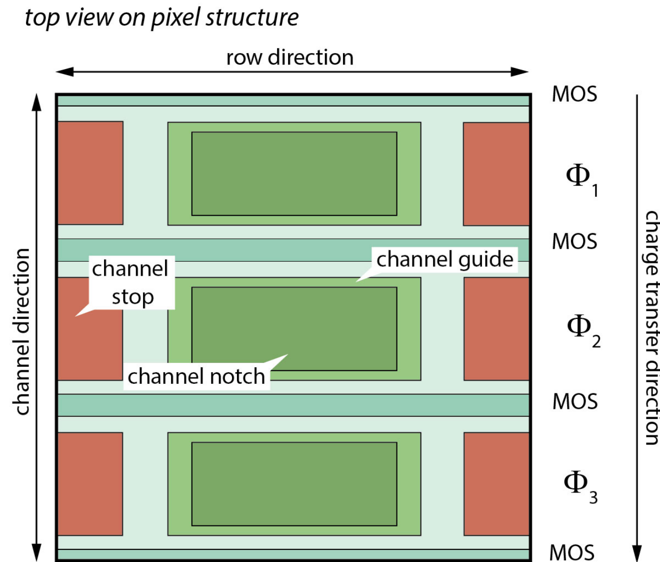

Figure 3.3: Structure of a pnCCD pixel. The channels are definded by deep n-implants. In the center of the channel guides are additional n-implants, the so-called channel notches. The channel stop p-implants between the n-implants serve as additional potential barrier. The positive donor ions of the n-implants attract the signal electrons, whereas the negative acceptor ions of the p-doped channel stops repulse these electrons. Thus, the absence of the n-implant channel guides and channel notches forms a potential barrier along the channel direction. The MOS contacts between the p^+-shift registers improve the insulation between the registers. The channel stop implants serve as potential barrier between the channels in row direction.

Smaller n-implants are centered in the middle of the channel guides and define the narrow transfer channel notches along which the signal charges are shifted to the readout anode. The purpose of the channel notches is to improve the charge transfer properties. The channel notches concentrate the signal charges on a small volume so that they are shifted over fewer defects in the silicon during their transfer to the readout anode. This improves the charge transfer efficiency after radiation damages.
Thus, the electric potential at the front side of the pnCCD is defined by the register contacts, the MOS structure and the space charges in the depleted n- and p-type implants. The positive space charges of the depleted n-implants of channel notch and channel guide attract electrons, whereas the negative space charges of the depleted p-implant channel stops repulse electrons. So, channel notches and channel guides form local po-

tential minima for electrons, while the channel stops form local potential maxima.
In the channel direction, the electric potential is formed by the shift registers and MOS contact voltages. The signal charges can be collected and stored under one or two registers. For two register storage, the center of the potential minimum is below the MOS gate, which is located between two storage registers. The MOS structure improves the insulation between the p^+-registers by increasing the potential barrier between them. This enables large shift voltages to be applied to the p^+-registers, which increases the transfer properties. Furthermore, it attracts thermally generated electrons from surface defects and avoids their mixing with signal charges in the pixels.

3.2.2 Readout electronics

At the end of each channel, the signal charges are shifted to the readout anode. The anode is held on a more positive potential than the storage minimum of the channel notch and therefore forms a local potential minimum for signal electrons. Since the n-doped silicon around the readout anode is depleted, the anode is isolated from the other pnCCD contacts. The readout anode can be compared to a capacitor, which is charged with signal electrons. An aluminium contact connects the readout anode with the p-doped gate of the circular n-channel JFET (figure 3.4).

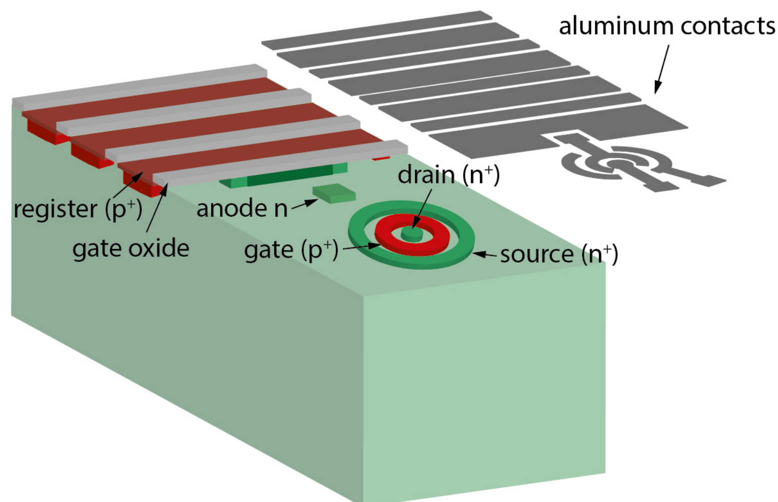

Figure 3.4: Readout region of the pnCCD. The aluminum contacts were removed from the last pixel, the readout anode and the first FET. The contact implantations of the first FET and the p^+-registers with the silicon oxide layers in between are visible.

Integrating the first FET on the pnCCD reduces the effective capacitance of the readout structure, consisting of the readout anode and the JFET gate. For a lower anode

capacitance, a given amount of charge on the anode is translated into a higher voltage swing on the first FET and thus results in a better signal-to-noise ratio. Since the JFET is located directly adjacent to the anode, its capacitance is kept small. This leads to high voltage signals of typically 2-3 $\frac{\mu V}{e^-}$, even for small amounts of charges. The JFET is operated in source follower mode and serves as impedance converter for signal amplification. The current source, which supplies the constant source-drain current through the JFET, is integrated in the readout chip CAMEX [15]. The JFET source voltage is further processed by the CAMEX ASIC. The differences in the voltage amplitude with and without signal, are amplified and transferred to a passive lowpass filter, which filters out high frequencies. Signal sampling is performed with an eight-fold correlated double sampling (CDS) filter. This filter samples the signal eight times and averages it before and after the signal electrons are shifted to the readout anode. Due to the high frequency noise, the fluctuations of the signal are reduced by approximately the square root of the number of samples. The CAMEX ASIC has 128 identical readout channels, which are processed in parallel. This enables low shaping times even at high readout rates.
During operation, the amplification factor (gain factor) can be adjusted through programmable CAMEX registers activating three switchable capacitors, which are part of the amplification circuit. By using a sample and hold stage after the CDS filter, the readout of the following row can already be performed during the multiplexing process of the current row. The multiplexer forwards the signal of all CAMEX channels into a differential output buffer. This output is connected to ADCs (Analog Digital Converters) that convert the analog signal into a digital one.

Summary of chapter 3

The basic topology and the working principle of the pnCCD have been introduced. pnCCDs are backside illuminated, three-phase CCDs on fully depleted silicon. In contrast to MOSCCDs, the transfer registers of the pnCCD are formed by pn-junctions. The potential wells, in which the signal electrons are stored, are formed by the register voltages and the space charges of the p- and n-implants of the pixel structure. The pnCCD has an on-chip electronics consisting of a readout anode and a monolithically integrated first FET at the end of each channel.

4 Numerical device simulations

Numerical device simulations help to get a better insight into the electrical conditions inside electronic devices and to interprete the experimental data. Therefore, the electric potential and the distribution of the mobile charge carriers in the pnCCD have been calculated statically and time dependent by two-dimensional numerical device simulations. The device model is based on the design data of the pnCCDs including the geometry and doping profiles.

4.1 The drift-diffusion model

All device simulations presented in this work were performed with the program system WIAS-TeSCA (Two-Dimensional Semi-Conductor Analysis Package) [20], [21]. TeSCA is a two-dimensional numerical device simulation tool developed by the Karl-Weierstraß-Institute for Applied Analysis and Stochastics (WIAS) in Berlin. With TeSCA, the electric potential and the charge carrier densities at a certain time can be determined. In order to describe the motion of electrons and holes in semiconductors, TeSCA uses the drift-diffusion model, whose basic equations were derived by van Roosbroeck under the conditions of Boltzmann statistics [22]. In this approximation, a local relationship between the electric field and the mean energy of the charge carriers is proposed. It is assumed that the charge carriers are in thermal equilibrium with the crystal lattice. Therefore, the semiconductor is thermally described by the lattice temperature. The system of equations of the drift-diffusion model consists of the Poisson's equation (equation (4.1)) and the continuity equations for electrons (equation (4.2)) and holes (equation (4.3)) [23]:

$$-\nabla\left(\varepsilon\nabla V\right) = q\left(p - n + N_D^+ - N_A^-\right) \tag{4.1}$$

$$\nabla\overrightarrow{J_n} = q\left(R - G\right) + q\frac{\partial n}{\partial t} \tag{4.2}$$

$$-\nabla\overrightarrow{J_p} = q\left(R - G\right) + q\frac{\partial p}{\partial t} \tag{4.3}$$

The three searched parameters are the electrostatic potential V, the electron density n and the hole density p. These parameters are a function of time and of two spatial coordinates x and y. Furthermore, $\varepsilon = \varepsilon_0 \cdot \varepsilon_r$ is the dielectric constant, q the elementary charge and n, p are the charge carrier densities. N_D^+ and N_A^- are the concentrations of the ionized donor and acceptor atoms, $\overrightarrow{J_p}$ and $\overrightarrow{J_n}$ are the current density vectors of electrons and holes and $R - G$ is the recombination-generation rate.
The electron or hole current densities can be written as a function of the electric field strength, respectively as gradient of the charge carrier density [24].

$$\overrightarrow{J_n} = qn\left(x\right)\mu_n\overrightarrow{E}\left(x\right) + qD_n\frac{\partial n}{\partial x} \tag{4.4}$$

$$\overrightarrow{J_p} = qn\left(x\right)\mu_p\overrightarrow{E}\left(x\right) + qD_p\frac{\partial p}{\partial x} \tag{4.5}$$

μ_n, μ_p are the electron or hole mobilities and D_n, D_p are the diffusion coefficients for electrons respectively holes.
The Einstein relation (equation (4.6)) connects the diffusion coefficient with the particle mobility.

$$D = \mu\frac{kT}{q} \tag{4.6}$$

Thus, the current density consists of a drift term, describing the dependency of the electric field strength and a diffusion term, representing the dependency of the charge carrier density. The total current density (equation (4.7)) is therefore:

$$\overrightarrow{J} = \overrightarrow{J_n} + \overrightarrow{J_p} \tag{4.7}$$

The van Roosbroeck equations [22] occur as a system of non-linear partial differential equations. In order to solve them, mathematical models must provide the intrinsic carrier density, the mobility as well as the recombination and generation of charge carriers. The solutions of the semiconductor equations are only distinct after setting the boundary conditions. Dirichlet boundary conditions were used for the metal contacts of the registers and for the back contact, which means that the electric potential is specified at the boundaries. Those contacts are defined by the applied external voltage. The MOS

contacts are treated similarly, but the effects due to the oxide charges were included. At the oxide, a fixed electric field was assumed [25]. For the right- and left-hand borders of the simulated region of the periodic structure, Neumann boundary conditions were applied. Neumann boundary conditions mean that the normal derivative of the electric potential is specified at the boundaries. So, the electric field and the currents were assumed to be zero. The electric contacts are assumed to be ideal ohmic contacts.
The partial differential equations are solved using the Finite Element Method (FEM). For this purpose, the simulated region is spatially discretized on a two-dimensional, triangular Delaunay grid [26]. The time interval is subdivided into individual time steps. Because of the discretization, the semiconductor equations are converted into a non-linear algebraic system of equations, which is solved by applying the Gummel [27] or the Newton iteration [28]. Since the computing time increases with increasing number of grid points, it was made use of the symmetry properties of the pnCCD pixel structure and of local mesh refinements according to doping gradients [29].

4.2 Modeling of the pnCCD pixel structure

4.2.1 Process simulation

In semiconductor process simulations, the fabrication steps of the device like ion implantation, annealing, etching, deposition and oxidation are modelled. The results of the process simulations are the geometry and the distribution of fixed space charges. The basic process steps are implemented in the form of mathematical models. This enables testing different process parameters and to find the optimal settings for device processing. So, cost and time in device development can be reduced.
In this thesis, two different approaches are used for the modelling of the fabrication process. In the first one, the fabrication flow was simulated with the simulation tool Sentaurus Process from Synopsys [30]. This tool provides different implantation and diffusion models and the possibility to calculate implantation profiles statistically with Monte Carlo methods. In this approach, the dopant distribution is simulated by tracking the scattering of the individual dopants within the crystal lattice. By correctly accounting for the ion energy losses, the final doping distribution is estimated. Since this method describes the lattice orientation-dependent channeling better than analytical models, it was used in this study. The simulated doping profiles were cross-checked with SIMS (Secondary Ion Mass Spectroscopy) and SRP (Spreading Resistance Profiling) measurements, which are used to monitor the production process of the pnCCDs.

An essential step in the simulation of the device geometry by means of FEM is the calculation of the grid. The grid is necessary to discretize the continuous structure in order to calculate the device properties by the finite element method. The quality of the grid decides about the accuracy of the simulation and the computing time. Grid refinement is performed for regions of special interest, for example doping transitions.
To cross-check the simulation results with different approaches and algorithms, the device simulations were performed with the tools Sentaurus Device from Synopsys [31] and TeSCA. In Synopsys, the process parameters were obtained from the Sentaurus Process simulation, whereas in TeSCA, the implantation profiles derived from SIMS and SRP measurements were loaded into the grid. The results were the same with both simulation tools. In the following sections, the results of the simulations with TeSCA are presented.

4.2.2 Simulation region

In the pixel array of the pnCCD, the structure of a single pixel is repeated in both the channel direction and the row direction (figure 3.3). A device simulation performed on a region that covers three by three pixels is therefore sufficient to study the charge handling capacity and the charge transfer process. In order to approximate the electric potential and the density distribution of signal charges in three dimensions, two different two-dimensional simulations are needed. The first one represents a cut along the channel direction, while the other cut follows the row direction perpendicular to the channel direction (figure 4.1).
The simulation tool assumes that the structure of the third dimension is infinite. As the pixel structure is repetitive in the channel and the row direction, three-dimensional effects only play a minor role for cuts in these directions and can be neglected (section 5.3). Due to the complexity of the structure and the size of the simulation region, the parameter space that could be tested would be extremely limited for three-dimensional simulations because of the high computation time. Three-dimensional simulations were only performed for a choice of parameter settings to check the results of the two-dimensional simulations. They were realized with the Sentaurus Device simulator. They showed, that the influence of the third dimension for a two-dimensional cut in the channel direction does not effect the characteristic of the electric potential. The deviation between the total value of the electric potential for two-dimensional and three-dimensional simulations is only in the range of a few 100 mV (section 5.3).

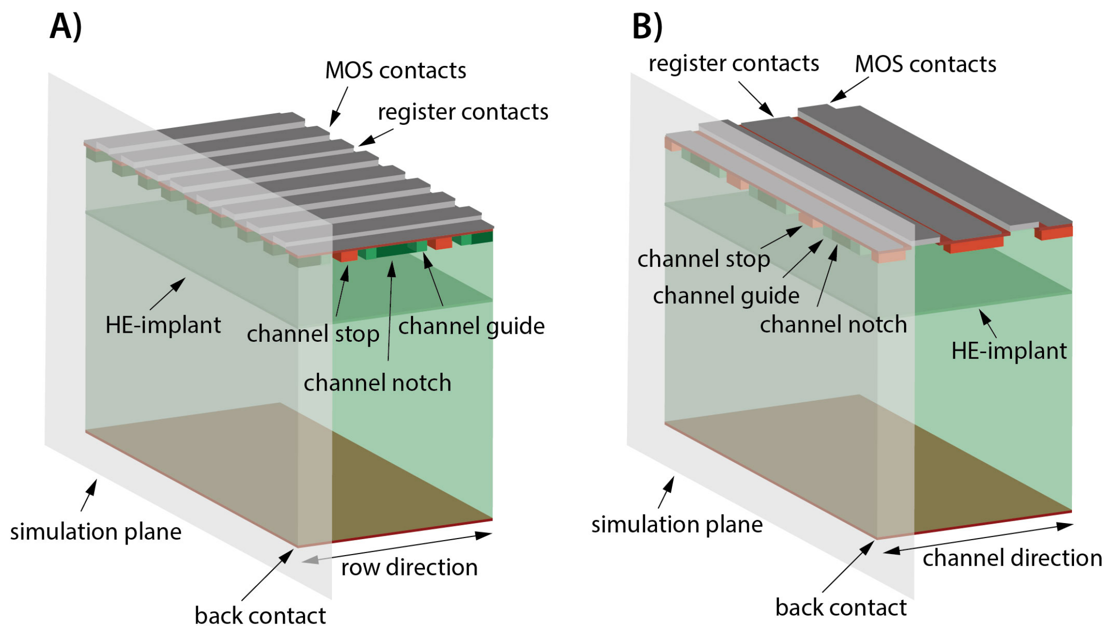

Figure 4.1: Cuts through the pnCCD in the channel and the row direction. A) Cut through the middle of a channel guide along the channel direction. The simulated region covers three pixels, corresponding to nine registers. It is symmetrical to the register in the center. B) Cut through the middle of a register along the row direction. The region has a width of three pixels. It is symmetrical to the channel guide implant in the pixel center.

This is due to the weak influence of the channel stop implants on the electric potential at the middle of the channel notch implants. For simulations in the row direction, the influence of the MOS contacts and the neighboring transfer registers on the electric potential of the simulated transfer register can not be modelled. The voltage of the MOS contacts and the adjacent registers is constant over the whole pixel area and therefore its influence on the region of channel notch and channel stop is the same. Only the difference between the electric potential at the location of the implants of channel notch and channel stop depending on the applied register voltage is essential for our considerations concerning the pixel full well capacity. If the applied MOS voltage was simulated, it would shift the electric potential of both regions by the same value. Only the voltage offset would be changed. The difference of the electric potential between channel notch and channel stop would not be affected.
For simulations in the channel direction, the cut is performed through the middle of the channel notch (figure 4.2). The simulation in the row direction is performed through the middle of the transfer register (figure 4.3). In both cases, the width of the simulated region is three pixels with a pixel size of $75\,\mu\text{m} \times 75\,\mu\text{m}$. This corresponds to nine

registers in the channel direction.
In figure 4.2 and figure 4.3, the pixel structure is depicted without the aluminium contacts and p^+-register implants. The n-doped regions are green and the p-doped regions of the channel stop implants are red. The depth of the simulated region is 450 µm and corresponds thereby to the depth of the pnCCD. The pixel implants are at the register side and at a depth of 7 µm below the register side is the high-energy phosphorous implant (HE-implant). Additionally, there is a p-doped contact implant at the back side of the n-doped silicon.
Unless otherwise stated, pnCCDs with a pixel size of 75 µm × 75 µm were chosen for the simulations and measurements. pnCCDs with this pixel size provide a good spatial resolution and a high charge handling capacity simultaneously. For this reason, pnCCDs with this pixel size have already been used in many projects, such as in the CFEL ASG Multi-Purpose (CAMP) chamber at the Linac Coherent Light Source (LCLS) of the Stanford Linear Accelerator Center (SLAC) [3].
The simulated depth is equal to the device thickness of 450 µm. The electric potential of the transfer registers and the back contact are defined by the applied external voltages. At the MOS contacts, the electric field in the oxide layer is generated by the aluminum contact voltage and the fixed oxide charges located at the interfae between the oxide and the silicon. It defines the electric field at the silicon-oxide interface. The normal vector components of the electric field, as well as of the electron and hole current densities, are assumed to be zero at the interface.
In order to complete the device model, implantation profiles are loaded into the grid. The bulk doping of the wafers was calculated from their depletion voltage using equation (2.2). The electric contacts in the simulation region are the back contact, MOS contacts and the register contacts, consisting of a Φ-offset value and a Φ-amplitude. Since, in the row direction, the cut for the two-dimensional TeSCA simulation goes through the middle of a transfer register, the influence of the MOS contacts and the neighboring transfer registers is not simulated. Their influence was derived from the results of the three-dimensional simulations (section 5.3).

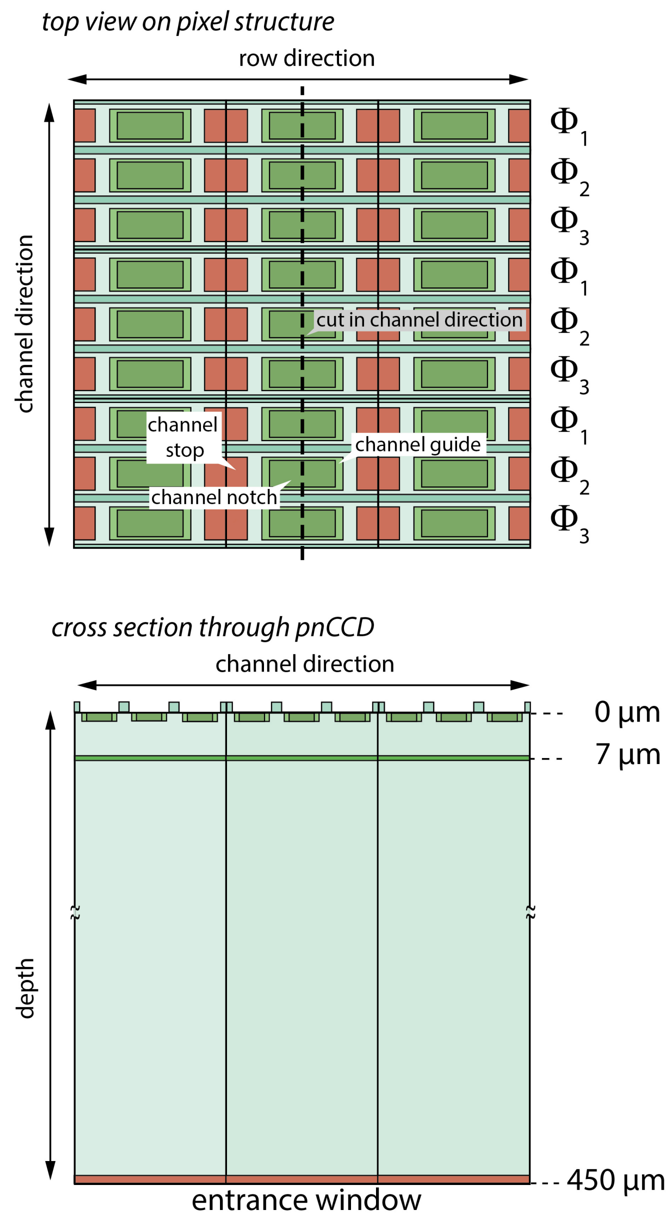

Figure 4.2: Top view and cross section of the simulation region in the channel direction. The pnCCD device is cut through the middle of the pixels in the channel direction, which is the middle of the channel notch. The locations of the implants are highlighted in different colors. The p^{+}-implants of the channel stops and the back contact are colored red, the n-doped silicon bulk is light green and the n^{+}-implants of the high-energy phosphorous implantation and the channel implants are dark green.

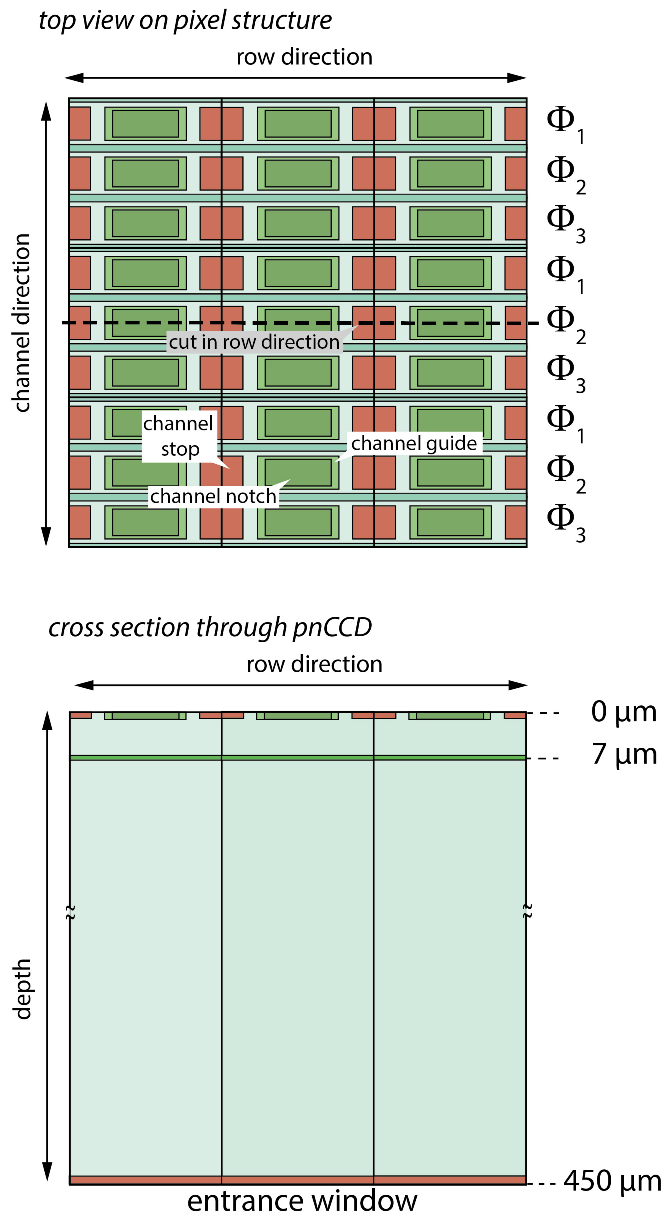

Figure 4.3: Top view and cross section of the simulated part of the pnCCD in the row direction. Depicted are the top view and the cross section of three pixels in the row direction. The cut follows the middle of the pixels in the row direction, which is the middle of the transfer register. The p^+-implants are colored red, the doped bulk is light green and the n^+-implants at the register side are dark green, as well as the high-energy phosphorous implant.

4.3 Modelling of the charge collection process

4.3.1 Charge collection

In TeSCA, the detection of photons is simulated by the injection of charge carriers, both electrons and holes, at the position in the simulation region where the photon would

have generated an electron-hole cloud. Therefore, the actual charge generation process is not simulated. The position and the number of electrons and holes can be chosen to match the energy of the simulated photon (figure 4.4). Consequently, the complete process, starting from charge collection - diffusion and drift - to charge transfer, can be modelled. The initial parameters are the number of generated charges, the coordinates where the charges are generated and the charge distribution of the electron-hole cloud. The charge carrier motion to their potential minima is calculated as a superpostion of drift, diffusion and electrostatic repulsion. The systematic motion of the charge carriers in the electric field is superimposed by the random motion due to the thermal energy of the electrons and holes. The arora mobility model [20], [32] is used for the simulation of the electron and hole mobility.

The drift of the signal electrons in a pnCCD can be divided into two phases. In the first phase, the charge cloud drifts in a homogeneous field towards the potential minimum of the register side and expands due to diffusion and electrostatic repulsion. The maximum electrostatic repulsion occurs right after the electron cloud has separated from the holes, since at this time the net charge density is the highest. The second phase starts as soon as the electrons have reached a certain depth below the register side, the so-called separation depth. When an electron cloud reaches the separation depth, the lateral field component of the register structure has an effect on the charge cloud. The charges are than either collected in one storage cell or the charge cloud is split at the pixel borders in two neighboring pixels. They are influenced by the lateral field component of the register structure. The separation depth is approximately the size of a pixel [29].

In the experimental setup, the signal charges in the pnCCD are generated by an optical laser. According to the experiments, the charge carriers are inserted in the middle of the center pixel in the simulations. To determine the pixel full well capacity, the charge spilling into neighboring pixels is observed, while increasing the number of generated signal charges. The wavelength of the laser is 635 nm. One photon of this wavelength has an energy of 1.95 eV. The penetration depth at this wavelength is only a few 10^{-6} m. The electrons are therefore generated close to the entrance window at the backside and have to drift over the complete detector thickness to get to the potential minima at the register side.

In the TeSCA simulations, a shorter drift distance is chosen. To study the charge handling capacity, the signal charges are generated in a depth of 20 µm below the register side. This ensures, that even at high amounts of signal charges, the charge distribution over the pixels takes place due to charge spilling into neighboring pixels and not due to the expansion of the charge cloud over pixel borders. In TeSCA, the calculation of the electrostatic repulsion in a two-dimensional plane is overestimated

[29]. For short drift distances, during which the charge cloud does not expand over the pixel border, the incorrect calculation of the charge cloud expansion is negligible for our considerations.

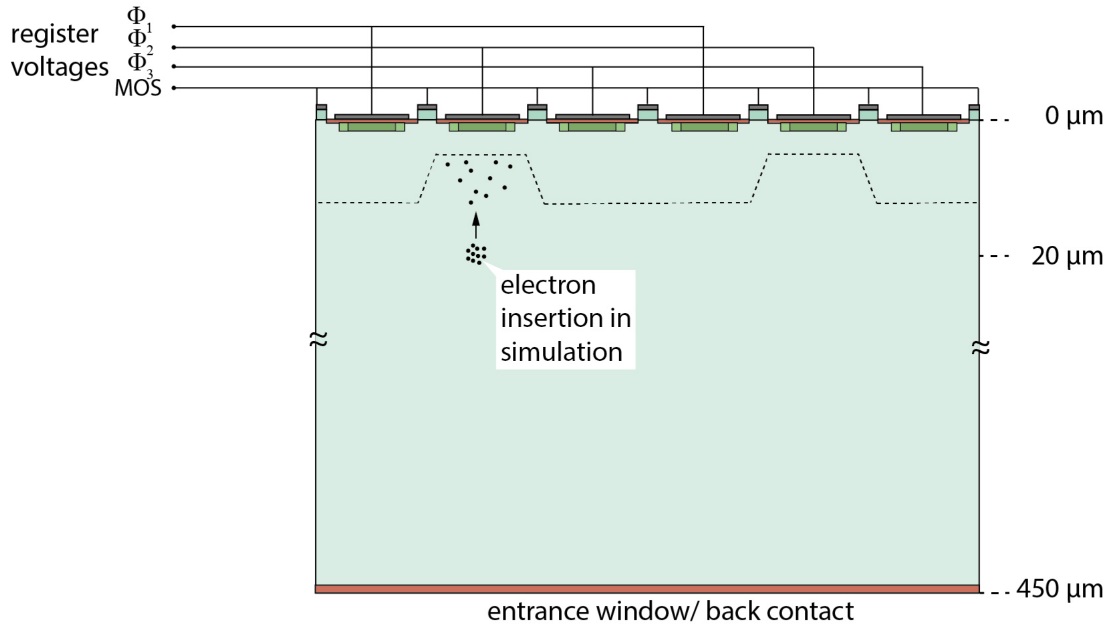

Figure 4.4: Cut through the middle of a channel guide along the channel direction. The depicted region covers two pixels consisting of six registers. It reaches from the register side to the back contact. The electrons are stored under one register. In the device simulation, the signal charges are generated in the silicon bulk at a depth of 20 µm below the register side and drift to the front contacts. Therefore, the drift distance of the signal electrons is shorter in the device simulation than it is in the experiment.

4.3.2 Charge storage

At the previously defined contacts, which are the back contact, MOS contact and the three register contacts Φ_1, Φ_2 and Φ_3, voltages can be applied for defined time intervals. This allows performing static simulations of the electric potential with constant voltages applied as during charge collection as well as changing the applied voltages periodically as during charge transfer. So, the charge transfer during which the register voltages are varied periodically can be simulated by defining time intervals during which the voltages have a well-defined value (figure 3.2). The charge collection process takes place within a period of several microseconds, which is sufficient to ensure that all signal electrons are accumulated in the potential wells and an equilibrium state is reached.
In the experiment, the signal electrons are stored under two registers. This means that

during integration time two of the three registers of each pixel are storage registers. The Φ-offset voltage is applied to the storage registers, whereas the sum of Φ-offset and Φ-amplitude is applied to the barrier registers. Therefore, the storage registers are on a more positive voltage than the barrier registers and attract electrons. After the charge collection, the electrons are shifted to the readout by a three-phase transfer. At a certain time of the transfer cycle, the entire charge is stored in one register only. In this state, the charge density is the highest, and thus the probability that some of the electrons spill into neighboring pixels is the greatest. For this reason, the simulations were performed for storage under one register to determine the pixel full well capacity.

4.3.3 Charge transfer

The number of signal electrons that are measured at the readout is not necessarily the number of signal electrons that can be stored in one pixel during integration time. During the shift to the readout anode, the electric potential of the pixel structure is periodically changed. The principle of a three-phase transfer in a CCD is shown schematically in figure 3.2. In the simulation, the register voltages are changed successively in 1 V steps. Initially, charge storage under one register is assumed. This means that every third register electrode of the pnCCD has the same potential during integration time. In this case, the storage registers are supplied with a more positive voltage than the two barrier registers. In figure 3.2, the initial storage register is called Φ_2 and the two barrier registers are called Φ_1 and Φ_3.
To simulate the charge transfer using TeSCA, the voltage of the barrier register that is adjacent to the storage register in charge transfer direction (Φ_3) is increased to more positive values in 1 V steps, until they have the same voltage as the storage register (Φ_2). The voltage of the storage register (Φ_2) is held constant. Now, two of the three registers are storage registers (Φ_2, Φ_3). Thus, the voltage of the initially storage register (Φ_2) is lowered to more negative values in 1 V steps, until it has the same voltage as a barrier register. All signal charges are now shifted to the next register. In the next step, the signal charges are transferred to the next register Φ_1 in the same way. In this way, the electrons are transferred from one pixel to another and the charge losses during the charge transfer process are observed to obtain the amount of signal electrons that reaches the readout anode.

Summary of chapter 4

The principle of the two-dimensional numerical device simulations used in this work has been introduced. They are based on the solution of the drift-diffusion model consisting of the Poisson's equation in electrostatics and the continuity equations for electrons and holes. The electric potential and the density distribution of signal charges in three dimensions were approximated by two-dimensional simulations in the row direction and in the channel direction. The simulations of charge collection, storage and transfer were performed with the tools WIAS-TeSCA and the Sentaurus Device simulator.

5 Electric potential in the pnCCD pixel

In order to characterize the electric potential inside a three-dimensional device using two-dimensional device simulations, two different simulations are used. The first one describes the distribution of the electric potential through a cut in the channel direction, while the other cut follows the row direction. This chapter gives a short introduction to the visualization of the simulation results, which are two-dimensional and one-dimensional cuts through the electric potential. The physical meaning of the simulation results is presented in the following chapter.

5.1 Electric potential in the channel direction

In the pixel array of a pnCCD, the basic pixel structure is repetitive in both, the channel and the row direction. Because of the periodic structure, a device simulation of a section covering three by three pixels is sufficient to describe the whole pixel area (section 4.2.2).

Figure 5.1 shows the electric potential of three pixels for a cut in the channel direction. In the channel direction, each pixel is divided into three registers. The simulation plane reaches from the register side to the back side at a depth of 450 µm and thus covers the entire thickness of the device. The cut is made in the channel direction through the middle of the channel notch (figure 4.2). The third dimension is assumed to be infinite and to have no influence on the simulation results. The applied boundary conditions (section 4.1) guarantee that the solution of the electric potential is valid and periodic at the borders of the simulation region. At the electric contacts of the back side and register side, the contact voltage is the boundary condition.

For the simulation of figure 5.1, the standard operation conditions for spectroscopy are applied. There were no signal charges injected. The back contact, which is located at a depth of 450 µm, is set to -230 V. The inner substrate contact at the opposite register side is defined as zero. At the register side, the structure of the nine transfer registers is clearly visible. The Φ_2-registers, which are in the center of each pixel, are the storage registers. They form local potential minima for electrons. The Φ_1- and Φ_3-registers form electric potential barriers for electrons.

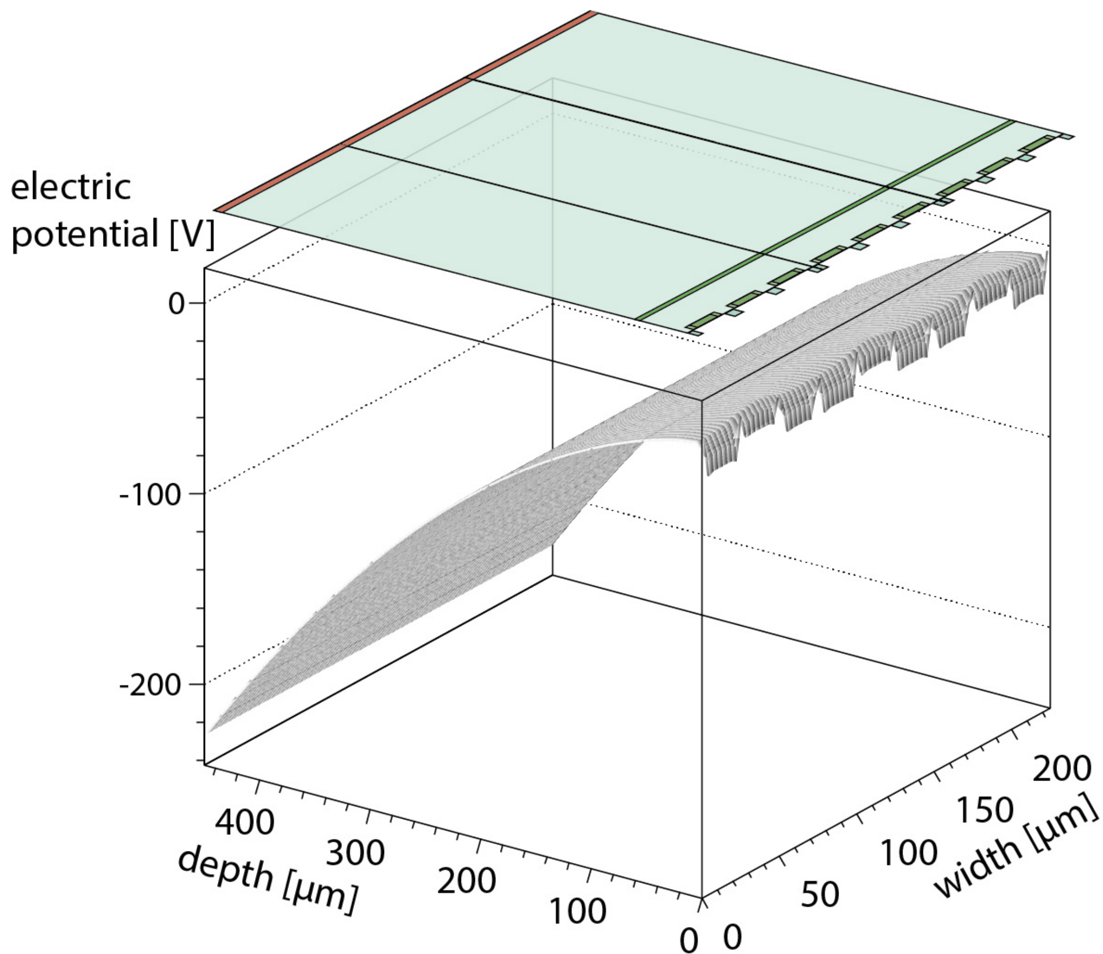

Figure 5.1: Electric potential in the channel direction. Electric potential of a two-dimensional simulation in the channel direction. The electric potential of three pixels is plotted as a function of the depth and of the width of the simulated region. The storage register is on a more positive potential than the two barrier registers. The voltage of the MOS contacts between the transfer registers are set to 0 V and voltage of the back contact to -230 V as used for standard operation mode. The pixel geometry of the simulated region is depicted above the plot of the electric potential.

In figure 5.2, the electric potential of two registers in the channel direction is plotted from the register side to a depth of 20 µm. The storage register is set to an offset value of -18 V, while on the two barrier registers of each pixel, the sum of Φ-offset (-18 V) and Φ-amplitude (-9 V), which is -27 V, is applied.

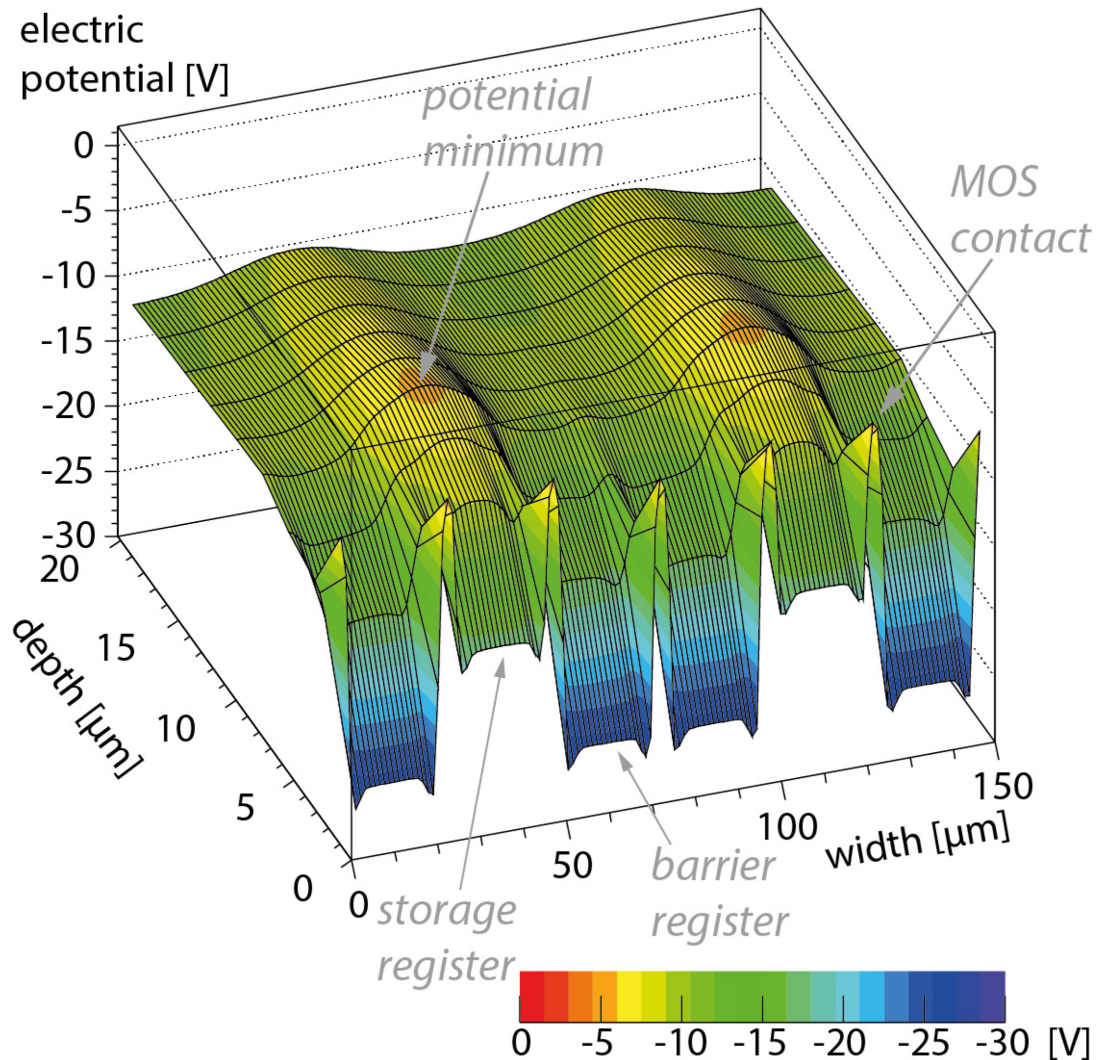

Figure 5.2: Electric potential of two pixels in the channel direction. The color code shows that the storage register is on a more positive potential than the two barrier registers. The MOS registers between the transfer registers are set to 0 V and the back contact to -230 V. The potential minimum is at a depth of 7 µm under the storage register.

The MOS contacts define the electric potential at the surface between the p^+-registers. They are set to 0 V. The MOS contacts improve the insulation between the p^+-registers. The positive space charges of the depleted n-silicon between the transfer registers create

a small potential barrier for holes. This potential barrier can be increased by applying a voltage of 0 V to the MOS contacts between the transfer registers. The MOS contacts are then operated in accumulation (figure 2.2B). In standard operation mode, the potential minimum and therefore the storage depth for electrons is at a depth of 7 µm below the register side, which is the depth of the high-energy phosphorous implantation (figure 5.2).

For a better insight in the potential structure, the electric potential in figure 5.2 is rotated. The rotated view of the electric potential of two pixels from the register side to a depth of 20 µm is shown in figure 5.3.

The peaks in the electric potential, which are located at the edges of the transfer registers, are generated by the different doping of the channel guide and channel notch. The colored lines in figure 5.3 represent the position of the cuts through the middle of the storage register, barrier register and the MOS contact between the storage and the barrier register as well as the MOS contact between two barrier registers plotted in figure 5.4.

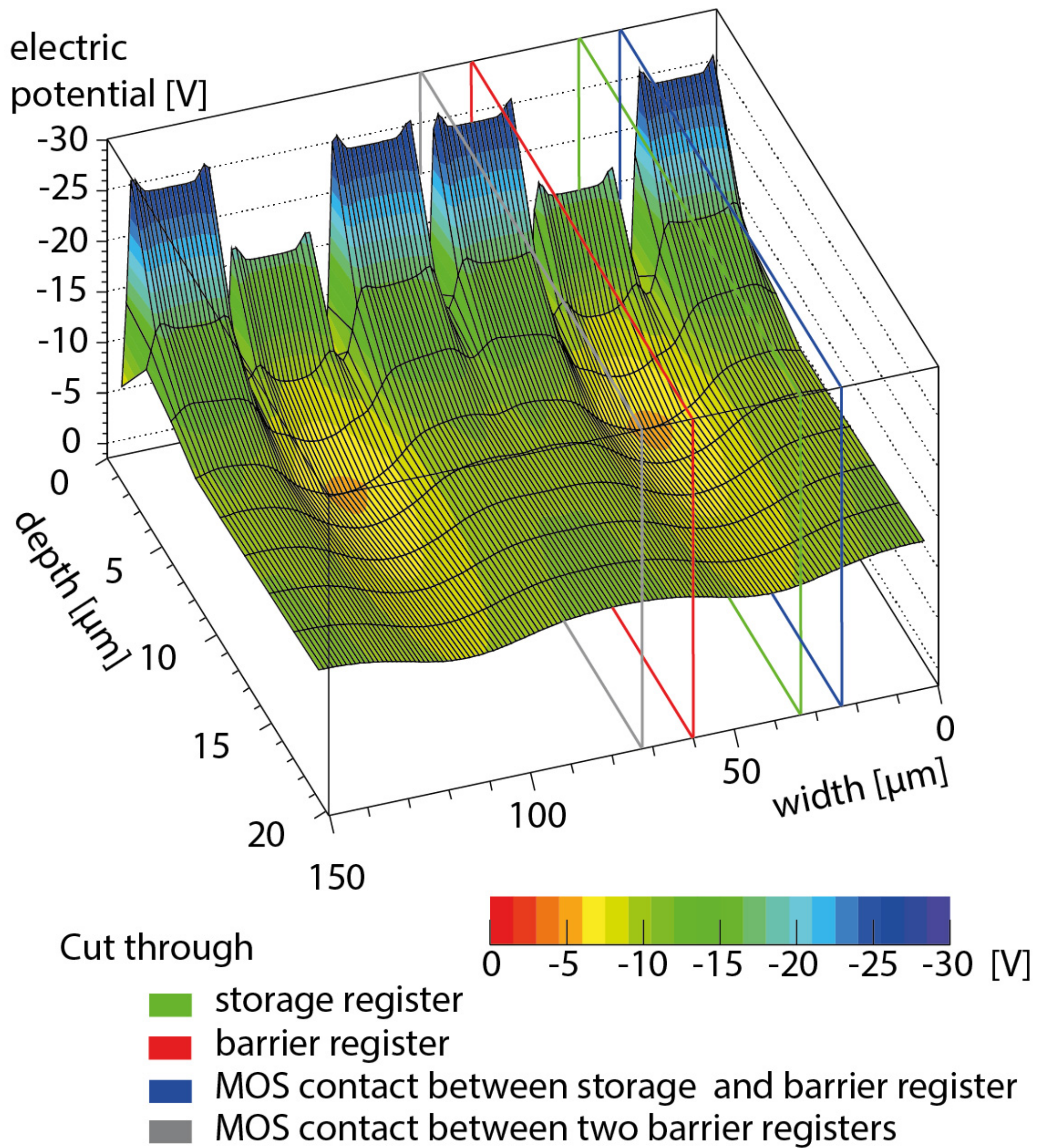

Figure 5.3: Rotated view of the electric potential of two pixels in the channel direction. The colored lines represent cuts through the middle of the storage register, barrier register and the MOS contact between the storage and barrier register as well as the MOS contact between two barrier registers. The peaks in the potential, which are located at the register side, are generated by the different doping of channel guide and channel notch.

The curves in figure 5.4 are one-dimensional cuts through the two-dimensional simulation of the electric potential in the channel direction. They show that there is a global potential minimum for electrons at a depth of 7 µm, which is defined by the high-energy boron implantation of the transfer channel. Located at a depth of approximately 1 µm is the transition from the n-implants of the pixel structure to the weakly n-doped (n^-) silicon bulk. The potential barrier between storage and barrier register at a depth of 7 µm is approximately 5 V.

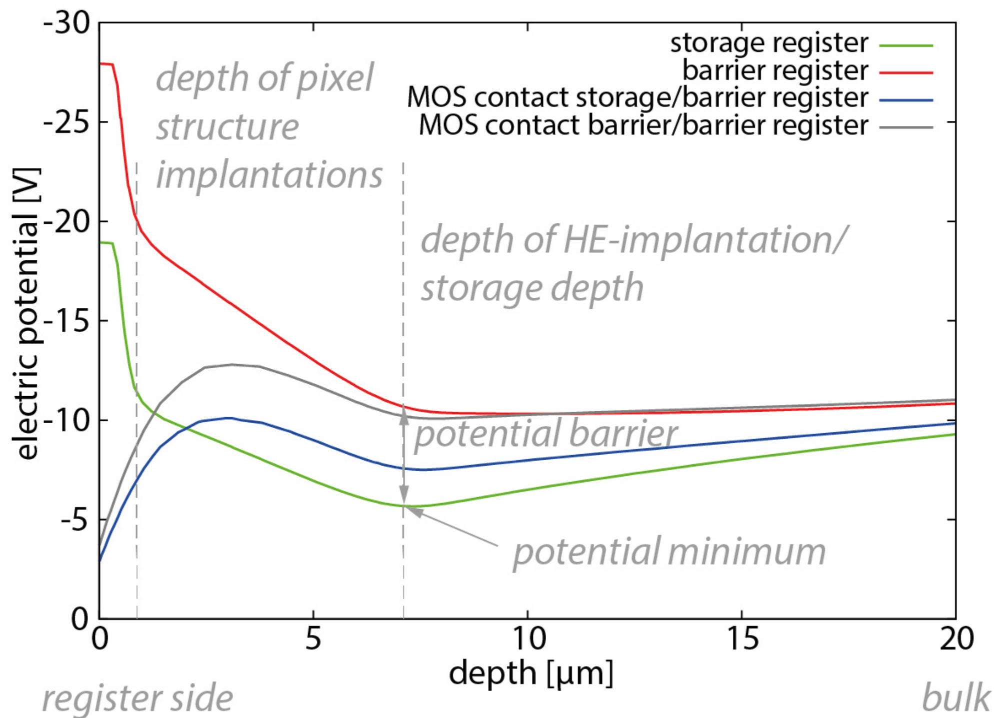

Figure 5.4: Cuts through the electric potential in the channel direction. One-dimensional cuts through the two-dimensional simulation of the electric potential in the channel direction. The cuts are performed through the middle of the storage register, the barrier register and the MOS register, between storage and barrier register as well as between two barrier registers. They are plotted to a depth of 20 µm. The implantations of the pixel structure are at a depth of approximately 1 µm and the high-energy implantation is at a depth of 7 µm below the register side. The global potential minimum for electrons is at a depth of 7 µm under the storage register.

The kink in the electric potential near the register side is due to the limited density of grid points. Although both MOS contacts have the same contact voltage, their electric potential profile differs. The electric potential of the adjacent registers influences the electric potential profile under the MOS contacts and vice versa. The electric potential of the barrier registers is more negative as of the storage registers and therefore

pushes the electric potential of the MOS register between two barrier registers to more negative values than the MOS register between a storage and a barrier register. In the simulations, the register side at a depth of 0 µm is defined as the surface of the silicon wafer. At the region of the MOS contacts, this corresponds to the interface between silicon and silicon oxide. However, the MOS voltage, which is 0 V, is applied on the silicon oxide. Therefore, the voltage at the register side depicted in figure 5.3 is not 0 V. The curves have to be extrapolated over the silicon oxide to reach the applied MOS voltage of 0 V.

5.2 Electric potential profile in the row direction

According to the simulations in the channel direction, the electric potential distribution of three adjacent pixels in the row direction is shown in figure 5.5. The cut in the row direction reaches across the whole detector thickness, from the register side to a depth of 450 µm. In the row direction, the n-implants of channel guide and channel notch define the pixel center and the p-implant channel stops define the pixel borders (figure 4.3).

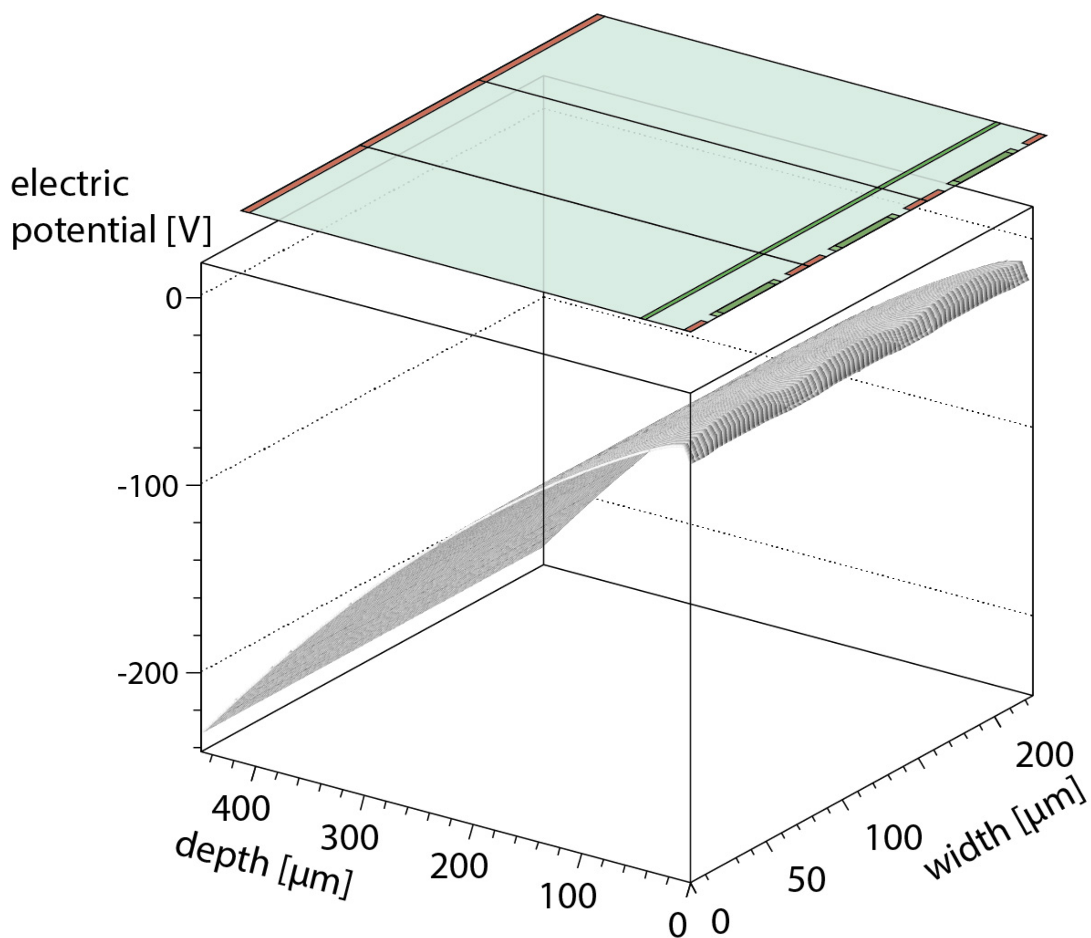

Figure 5.5: Electric potential in the row direction. Two-dimensional simulation of the electric potential in the row direction. The electric potential of three pixels is plotted in dependence of the depth and of the width of the simulated region. The channel guides and channel notches are on a more positive potential than the channel stops due to the different doping of these regions. The register contact is set to -18 V and the back contact to -230 V.

The simulation represents a cut through the middle of a transfer register in the row direction. Since there is only one contact at the register side in the simulation in the row direction, which reaches over the whole width of the simulated region, either a storage or a barrier register can be simulated. The pnCCD is operated in overdepletion. Therefore, only the voltage offsets differ between a storage and a barrier register and not the principle course of the electric potential. The influence of the MOS contacts and the adjacent registers on the simulated register is not taken into account, as the third dimension is assumed to be infinite (section 4.2.2). Their influence is derived from the three-dimensional simulations (section 5.3).
Figure 5.5 shows the electric potential for a cut through a storage register for standard operation conditions used for spectroscopic applications. In contrast to the simulation in the channel direction, there are only two contact voltages applied. The back contact, which is at a depth of 450 µm, is set to -230 V. The opposite register side is set to -18 V, which corresponds to the Φ-offset value (section 5.1). The pixel structure in the row direction is not defined by the applied voltages, but by the pixel implantations. The positive space charges of the depleted n-implants of channel guide and channel notch attract electrons, while the negative space charges of the depleted p-implant channel stops repulse electrons. So, the channel guide and the channel notch form a potential minimum for electrons, whereas the channel stops form the potential barriers between adjacent pixels.

In figure 5.6, the electric potential of two pixels in the row direction is plotted from the register side to a depth of 20 µm. The potential minimum for electrons is at a depth of 7 µm below the register side at the middle of the channel notch. The steps in the electric potential at the junction between the channel middle and the channel borders are caused by the different doping of the channel notch and channel guide, respectively, channel guide and channel stop.

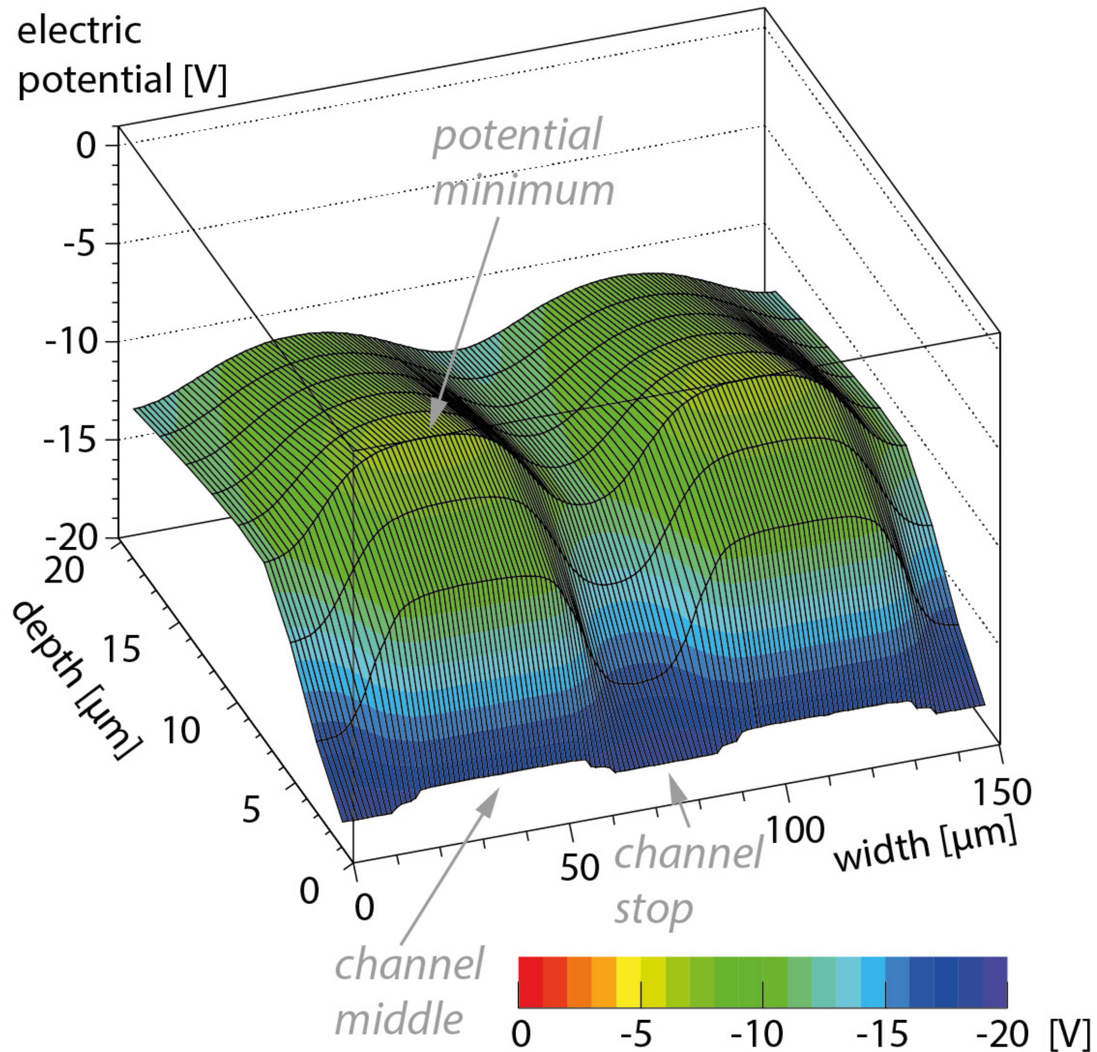

Figure 5.6: Electric potential of two pixels in the row direction. The color code shows that the channel middle is on a more positive potential than the channel stops. At the back contact are -230 V applied and -18 V are applied at the register contact. The potential minimum is at a depth of 7 µm under the channel middle.

The rotated view of the electric potential of two pixels from the register side to a depth of 20 µm is depicted in figure 5.7. The potential barriers between adjacent channels are exclusively generated by fixed depleted space charges, the channel stops. The electric potential of the channel stops is given by the depleted space charges and not by an externally applied voltage. Therefore, the potential barrier in the row direction can not be varied by voltages at the register side. It is fixed by the channel stop implants [13].

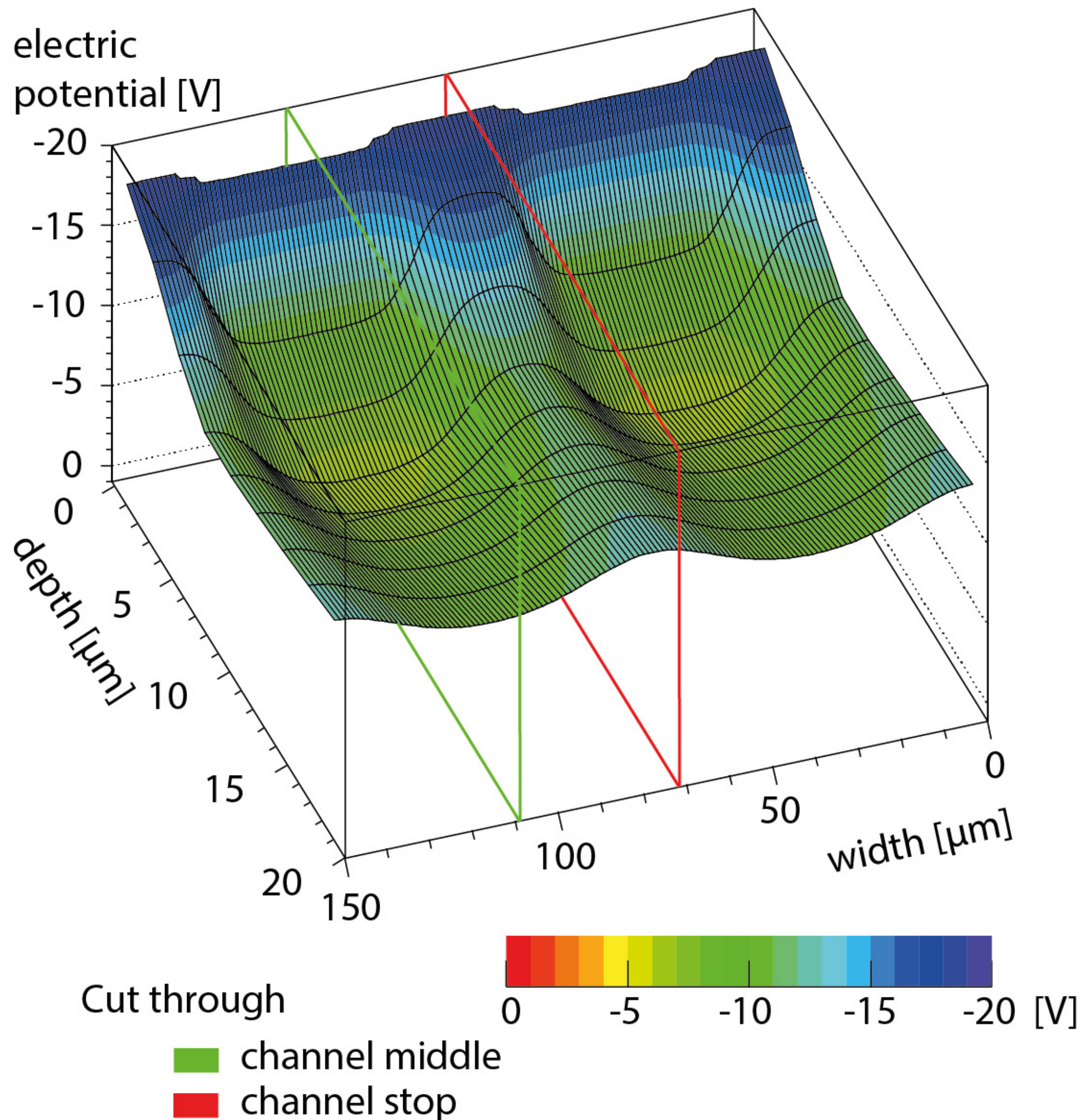

Figure 5.7: Rotated plot of the electric potential of two pixels in the row direction. The colored lines represent cuts through the middle of channel notch and channel stop.

In the channel direction, the potential barrier can be varied by the applied voltages of the barrier register and the MOS contacts. The colored lines in figure 5.7 represent cuts through the middle of the channel notch and channel stop.
The one-dimensional cuts in figure 5.8 show that there is a global potential minimum for electrons at a depth of 7 µm, which is defined by the high-energy boron implantation of the transfer channel. The transition from the n-implants of the pixel structure to the weakly n-doped (n^-) silicon bulk is located at a depth of approximately 1 µm. The potential barrier between channel notch and channel stop at a depth of 7 µm is approximately 5 V. The kink in the electric potential near the register side is here again owed to the limited density of grid points.

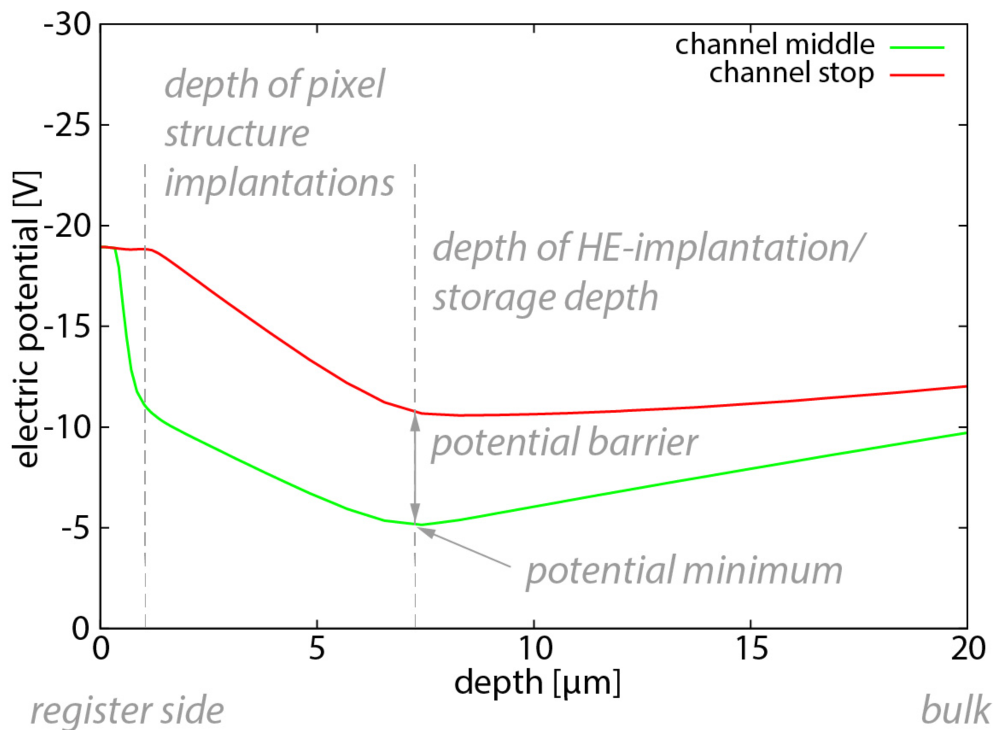

Figure 5.8: Cuts through the electric potential in the row direction. The plot shows one-dimensional cuts through the electric potential in the middle of channel notch and channel stop. The cuts are plotted to a depth of 20 µm. The implantations of the pixel structure are at a depth of approximately 1 µm and the high-energy implantation is at a depth of 7 µm. The storage depth for electrons is at a depth of 7 µm under the channel notch.

5.3 Electric potential in three-dimensional device simulations

In the two-dimensional simulations, the third dimension, which is not simulated, is assumed to be infinite (section 4.2.2). The cut for the two-dimensional simulation in the channel direction is performed through the middle of the channel notch (figure 4.2). For the simulation in the channel direction, the influence of the channel guide and channel stop implants in the row direction is neglected.
The two-dimensional simulation in the row direction is through the middle of a register, in our case a storage register (figure 4.3). Consequently, for a simulation in the row direction, the influence of the adjacent MOS contacts and transfer registers is not taken into account.
In the following, the deviation of the electric potential obtained from the simulation in two-dimensions from the three-dimensional simulations is studied.
The influence of the neglected channel guide and channel notch implants on the electric potential for a simulation in the channel direction is less than the influence of the neglected MOS contacts and transfer registers on the simulation in the row direction.
In the row direction, the difference of the electric potential between channel notch and channel guide is fixed by the ion implantations of these regions. The register voltage is applied to both implantation regions. Therefore, the voltage applied to the transfer register only adds an offset value.
However, in the channel direction, the difference of the electric potential between the storage and the barrier registers, respectively between the transfer registers and the MOS contacts varies with the voltages applied to the corresponding electric contacts.
In the previous sections of this chapter, it was shown that the potential barrier to the neighboring pixels obtained from the two-dimensional simulations in the row and the channel directions in standard operation mode is about the same. Comparing the electric potential for a cut in the channel direction with the related values of the three-dimensional simulations shows that the difference of the electric potential at the local potential minima is approximately 1 V or less. The course of the electric potential is identical to the two-dimensional simulations. The simulations only differ by an offset value (figure 5.9). Thus, the results of the two-dimensional simulations in the channel direction are in good agreement with the electric potential obtained from the three-dimensional simulations.

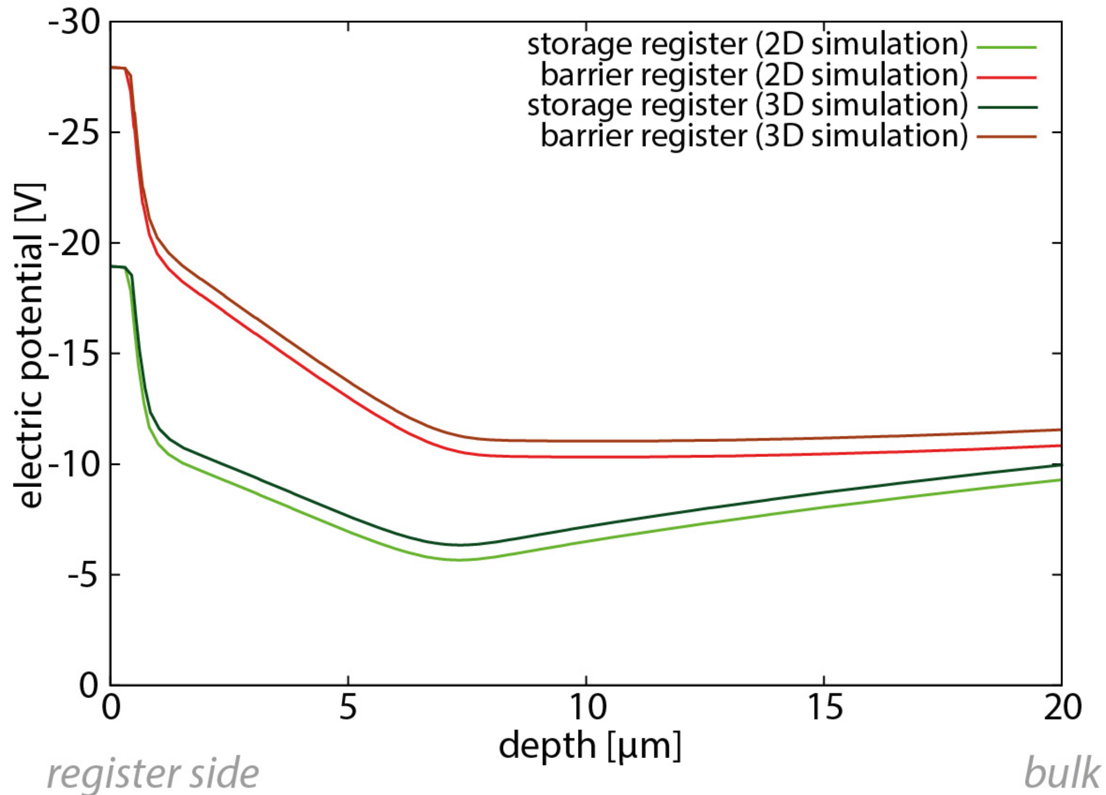

Figure 5.9: Electric potential for two-dimensional and three-dimensional simulations. The one-dimensional cuts are through the middle of the channel notch. The two-dimensional simulations are performed in the channel direction. The simulations in two and three dimensions only differ by an offset value caused by the electric potential in the third dimension, which is not simulated in two-dimensional simulations.

The reason is that the influence of the channel guide and channel stop ion implantations on the electric potential in the middle of the channel notch is low, compared to the influence of the voltages applied to the contacts of the transfer registers and MOS structure.
For simulation in the row direction, the difference of the electric potential of the two- and three-dimensional simulations is approximately 2 V or less. Here again, the course of the electric potential is identical to the two-dimensional simulations. The electric potential in the region of the channel notch resulting from the three-dimensional simulation is approximately 2 V more negative than for the two-dimensional simulations for storage under one register. The reason is that the operation voltage of the adjacent barrier register is at -27 V and therefore more negative than the storage register at -18 V. The more negative voltage of the neighboring barrier registers shifts the electric

potential of the storage register to more negative values in the three-dimensional simulations than in the case, when the storage register is assumed to be infinite.
The difference of the electric potential for a cut in the row direction between two- and three-dimensional simulations results in the fact that the potential barrier in the three-dimensional simulation is smaller in the row direction than in the channel direction in standard operation mode used for spectroscopy.
As presented in section 6.3.3, for the two-dimensional simulations, the potential barrier in the row direction is also smaller than the potential barrier in the channel direction, when the other tested parameters are used.
Since the differences in the electric potential for simulation in two- and three-dimensions is negligible small, two-dimensional numerical device simulations will be studied for the reasons mentioned in section 4.2.2.

Summary of chapter 5

A short introduction to the visualization of the two-dimensional device simulations and the one-dimensional cuts through the simulated electric potential in two-dimensions was given for different locations in the pixel structure. It was shown that the differences in the electric potential obtained from three- and two-dimensional simulations are negligible.

6 Electric potential during charge collection

The charge handling capacity of a pnCCD defines the maximum number of signal charges an individual pixel can hold. During charge collection, the applied voltages stay constant and form static potential wells in which the signal electrons accumulate during integration time. Afterwards, the signal electrons are shifted to the readout anode by periodically switching the register voltages. During charge transfer, signal charges can escape from the pixel in which they were collected, causing the so-called charge transfer losses.

In this chapter, the electric potential of the register side is studied during collection of the signal charges. The following factors have an effect on the electric potential: the operation voltages, the pixel geometry and the space charge distribution, as well as mobile charge carriers.

The dependency of the charge handling capacity on the pixel geometry and the space charge distribution is given by Poisson's equation in electrostatics:

$$\vec{\nabla}^2 \varphi = -\frac{\rho}{\varepsilon} \tag{6.1}$$

with

$$\rho = N_A + N_D + n_e + n_h + G - R \tag{6.2}$$

N_A and N_D are the concentration of acceptor and donor ions, n_e and n_h are the electron and hole concentration and G and R are the generation and recombination rate. Moreover, it can be written $\varepsilon = \varepsilon_0 \cdot \varepsilon_r$ with ε_0 being the vacuum permittivity and ε_r the relative static permittivity of the material.

6.1 Influence of the operation parameters on the electric potential

There are two ways to increase the charge handling capacity. The first is to increase the potential wells in which the signal charges are stored, respectively the height of the potential barrier that the electrons have to overcome to reach the neighboring pixels. The second is to decrease the storage depth of the signal electrons, which means decreasing the distance of the electrons from the nearest electrode.
pnCCDs are operated in overdepletion mode, such that the voltage applied across the detector exceeds the depletion voltage and the potential minimum is shifted to the register side. The potential minimum it is held at a depth of 7 µm by the high-energy phosphorous implantation. The charge handling capacity of a pixel can be compared to an electric capacitance [13], [33]. In this model, the pixel is represented by a parallel-plate capacitor. The register contact acts as the positive plate of the capacitor, whereas the negative plate is a virtual plane in the silicon at the depth where the signal electrons are stored. The capacitance C of a parallel-plate capacitor constructed of two parallel plates, both of an area A, separated by a distance d, is given by:

$$C = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{A}{d} \tag{6.3}$$

with ε_0 being the vacuum permittivity and ε_r the relative static permittivity. The pixel size and thus A is fixed. So, the reduction of the storage depth, here denoted as distance d, leads to an increase of the charge handling capacity. Additionally, there is a larger difference of the space charge distribution between channel notch and channel stop, since the effective implantation dose is higher closer to the wafer surface. The difference in the electric potential between channel notch and channel stop decreases with increasing storage depth. The space charge distribution of the device can only be changed during the production process.
After completion of the production process, the changes in the electric potential are achieved by the following parameters: the register voltages, the MOS voltage and the back contact voltage.

- **register voltages:** The register voltages determine the size and depth of the potential well and the location where the signal charges are stored. The register voltages consist of a Φ-amplitude and a Φ-offset. The Φ-amplitude determines the depth of the potential well. Reducing the Φ-offset voltage for a given back

contact voltage shifts the potential well closer to the surface, since the difference between the register side and the back contact is reduced.

- **MOS voltage:** The MOS structure defines the electric potential of the regions at the front side between the p^+-registers and acts as addtional potential barrier between the transfer registers. In standard operation mode used for spectrocopy, a MOS voltage of 0 V is applied and the MOS contacts are operated in accumulation (figure 2.2B). In accumulation, electrons, which are thermally generated by surface defects, are attracted by the silicon-silicon oxide interface under the MOS contacts. Therefore, they are prevented from drifting into the storage minima of the pixels, where they would mix with the signal electrons and degrade the spectrocopic perfomance of the device. If a negative voltage is applied to the MOS registers, the electrons are pushed away from the pnCCD surface and stay in their potential wells. This operation mode is called depletion (figure 2.2C). It is used for the high charge handling capacity mode. Since now the thermally generated charges also flow directly to the storage minima of the pixels, the spectroscopic perfomance is slightly degraded. However, the MOS registers cause a smaller modulation of the electric field than the p^+-registers, since the transfer registers are directly contacted pn-diodes. Furthermore, the width of the MOS registers is smaller than the width of the transfer registers.
- **back contact voltage:** The back contact voltage has an influence on the storage depth of the signal electrons. A more negative potential difference between the back contact voltage and the register voltages shifts the potential minimum of the electrons closer to the register side.

In figure 6.1, the above mentioned voltages are changed successively according to our considerations and the influence of the operation voltages on the electric potential is shown. To obtain optimal results, the voltages have to be adapted for each pnCCD. The following voltages are typical values, which are used to explain how the charge handling capacity can be increased by adjusting the operation voltages. The new set of operation parameters is called the high charge handling capacity mode (HCHC-mode). Figure 6.1 shows one-dimensional cuts through the simulation of the electric potential in the channel direction. The cuts are performed through the middle of the storage register, the barrier register and the MOS register between the storage and barrier registers as well as between two barrier registers. The resulting cuts through the electric potential are plotted to a depth of 20 µm.

Figure 6.1A shows cuts through the electric potential for standard operation mode used for spectroscopy. The back contact voltage is -230 V and the voltage of the MOS

registers is 0 V in standard operation mode. The Φ-offset voltage is -18 V and the Φ-amplitude is -9 V. The global potential minimum for signal electrons is at a depth of 7 µm, which is the depth of the high-energy phosphorous implantation. In this depth, the potential barrier between storage and barrier register is 5 V. Starting from these operation parameters, the depth of the potential well was increased by changing the register voltages.

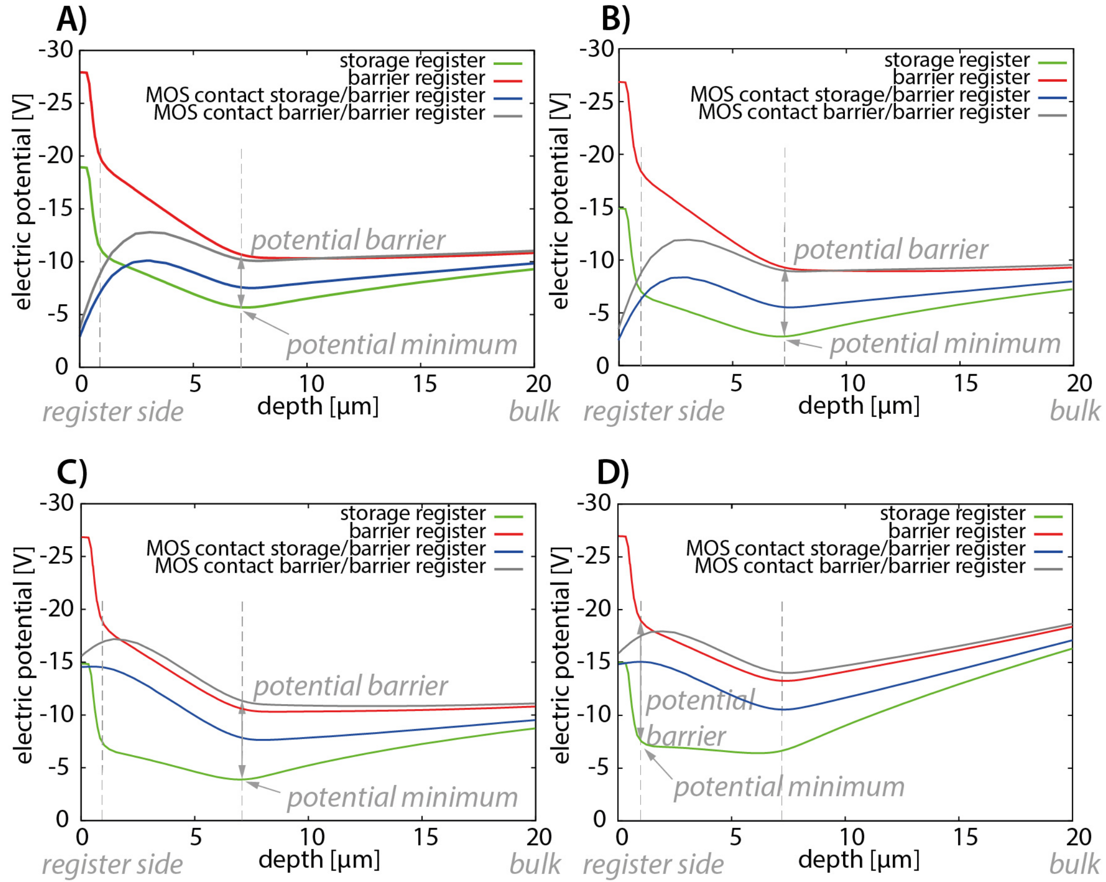

Figure 6.1: Influence of the operation voltages on the electric potential in the channel direction. Starting from the operation voltages of the standard operation mode (A), the register voltages (B), the MOS voltage (C) and back contact voltage (D) were changed. Thus, the potential barrier between the registers was increased and the storage depth was shifted closer to the surface.

As shown in figure 6.1B, the absolute value of the Φ-amplitude is increased from -9 V to -12 V to increase the potential barrier between storage and barrier register. The absolute value of the Φ-offset is decreased from -18 V to -14 V, so that the sum of Φ-offset and Φ-amplitude remains at about the same value.

In figure 6.1C, the voltage of the MOS contacts was lowered from 0 V to -15 V. A more

negative MOS voltage pushes the electrons away from the surface, so that they stay in their potential wells. The MOS contacts form an additional potential barrier for electrons between the p^+-registers, which the signal electrons have to overcome to get to the neighboring pixels. So, the potential barrier between neighboring pixels is increased by increasing the potential barrier between the storage register and the MOS register between the two barrier registers.

In figure 6.1D, the back contact voltage was set to -400 V. A more negative back contact voltage shifts the potential minimum at the depth of 7 µm to more negative values. At a certain value, the difference between the electric potential of global potential minimum at a depth of 7 µm and the electric potential at a depth of 1.4 µm is significantly reduced (figure 6.2). Most of the electrons overcome this small potential barrier and are now stored closer to the register side at a depth of 1.4 µm, which is the depth of the pixel implantations. At this depth, the potential barrier to the neighboring pixels is 11 V and therefore higher than it is at a depth of 7 µm.

By adjusting the operation voltages according to our considerations, the potential barrier between neighboring pixels was increased from 5 V to 11 V. The electric potential is more pronounced, which increases the charge handling capacity (figure 6.3). Furthermore, the storage depth was shifted from 7 µm to 1.4 µm below the register side. According to the model that compares the charge handling capacity to an electric capacitance, the number of electrons that can be stored in one pixel increases, if the storage depth is shifted closer to the register side.

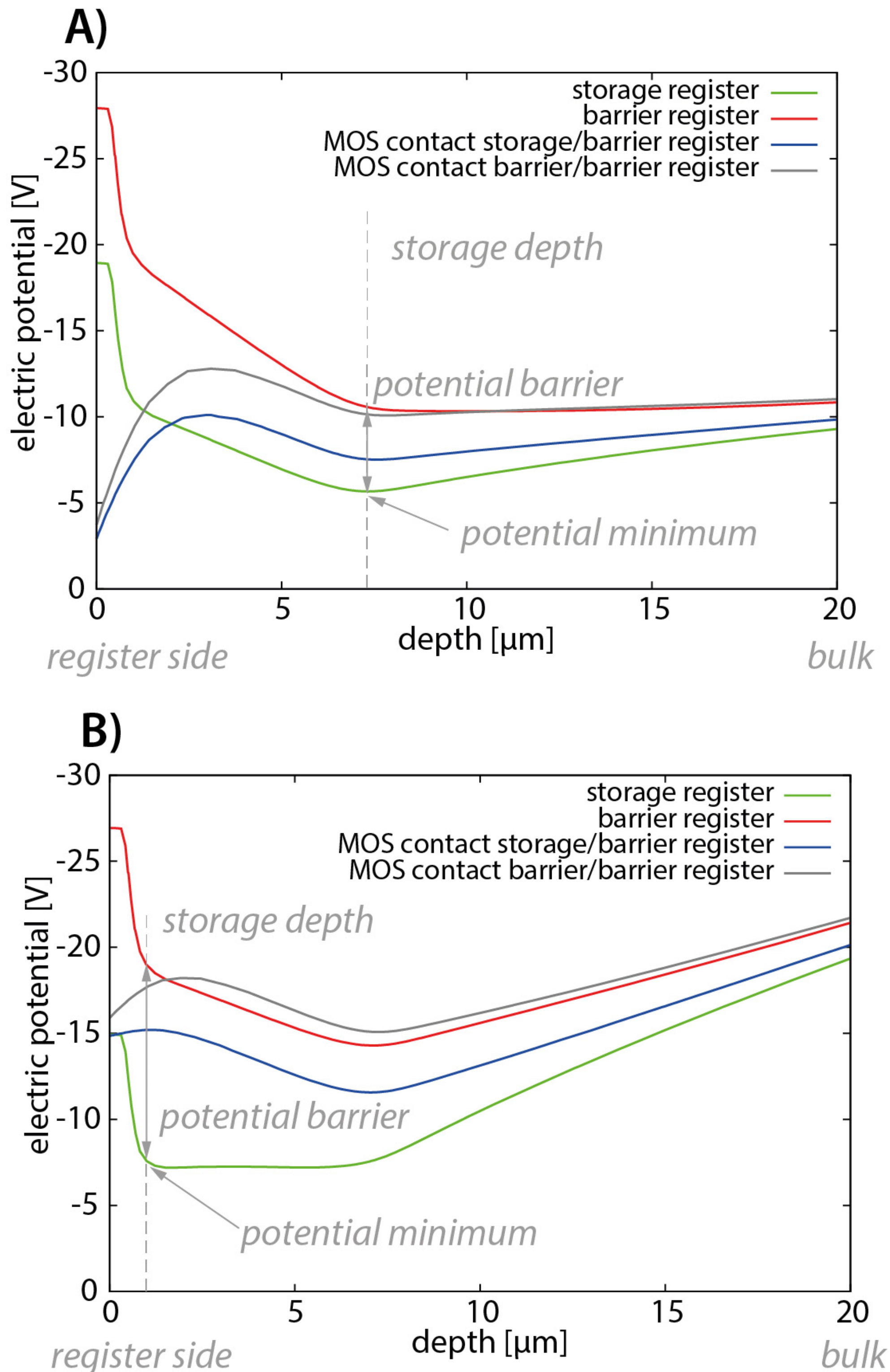

Figure 6.2: Cuts through the electric potential in the channel direction for standard operation mode and HCHC-mode. One-dimensional cuts through the electric potential of a two-dimensional simulation in the channel direction. The cuts are plotted to a depth of 20 μm. The potential minimum is shifted from a depth of approximately 7 μm under the storage register in the standard operation mode (A), to a depth of approximately 1.4 μm in the mode for high charge handling capacity (B). Furthermore, the potential barrier in the high charge handling capacity mode is higher than in the standard operation mode.

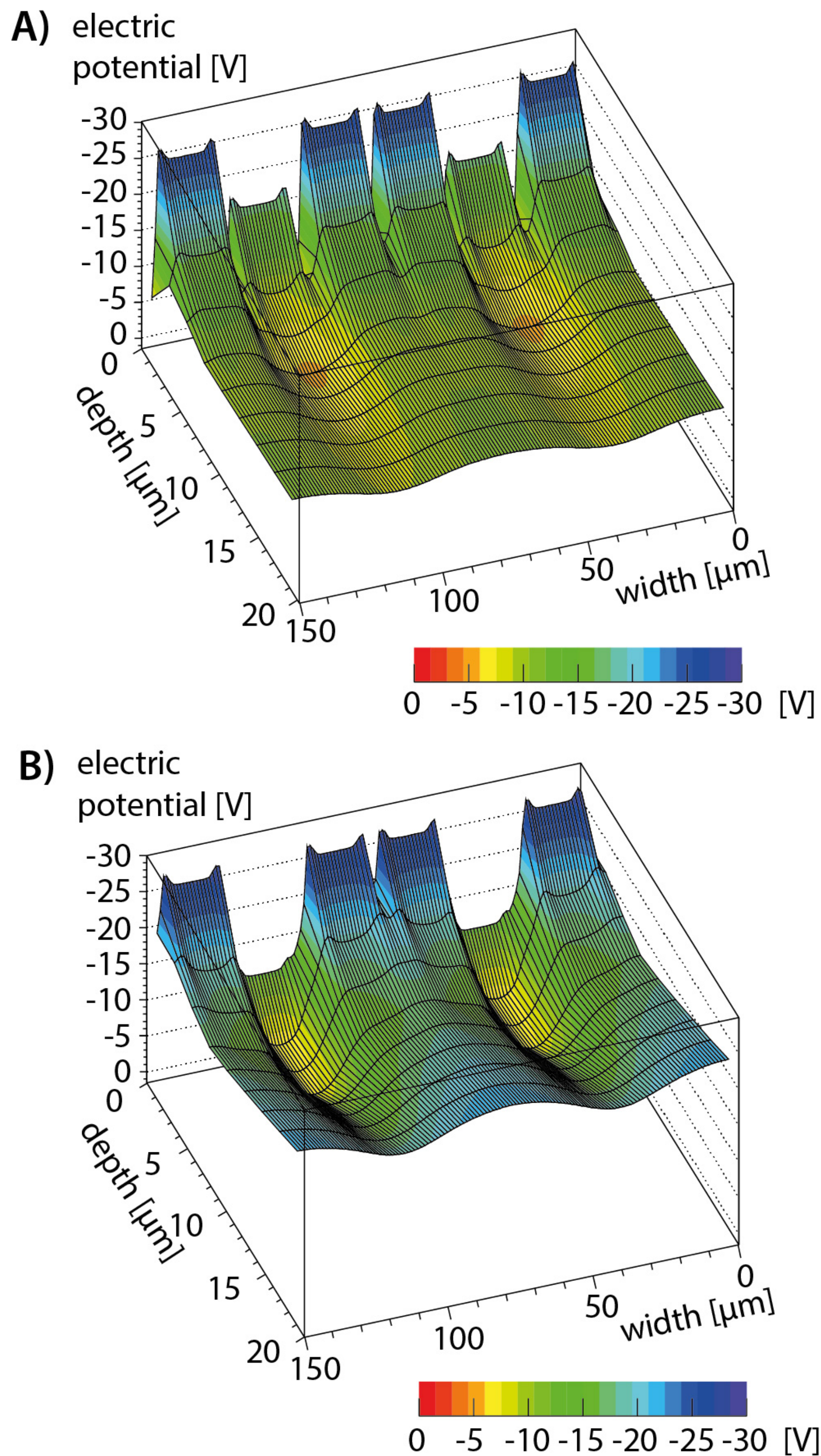

Figure 6.3: Electric potential in the channel direction for standard operation mode and HCHC-mode. The figures show the electric potential of two pixels from the register side to a depth of 20 µm. A) Electric potential in standard operation mode. B) Electric potential in operation mode with increased charge handling capacity. In the high charge handling capacity mode, the potential barriers are more pronounced and the storage depth is closer to the register side.

Figure 6.4 shows one-dimensional cuts through the two-dimensional simulation of the electric potential in the row the direction. The cuts were performed through the middle of the channel notch of the storage register, where the signal electrons are stored, and through the channel stop, which is the potential barrier to the neighboring pixels in the row direction. In figure 6.4A, the standard operation conditions, which are a Φ-offset voltage of -18 V and a back contact voltage -230 V, are applied. In figure 6.4B, the operation voltages for the high charge handling capacity mode with a Φ-offset voltage of -14 V and a back contact voltage -400 V are applied. The different Φ-offset values only lead to different voltage offsets, but they do not influence the principal course of the electric potential. However, applying a more negative back contact voltage in the high charge handling capacity mode reduces the difference of the electric potential at a depth of 1.4 µm and 7 µm, so that the electrons can be stored closer to the register side. This increases the pixel full well capacity compared to the standard operation mode. Since the potential barriers between adjacent pixels in the row direction are generated by the fixed depleted space charges of the channel stops, its height remains unaffected by the voltage changes. In the channel direction, the potential barrier to the neighboring pixels was significantly increased by the applied voltages in high charge handling capacity mode (figure 6.2). Therefore, the channel stops form the weaker potential barrier.

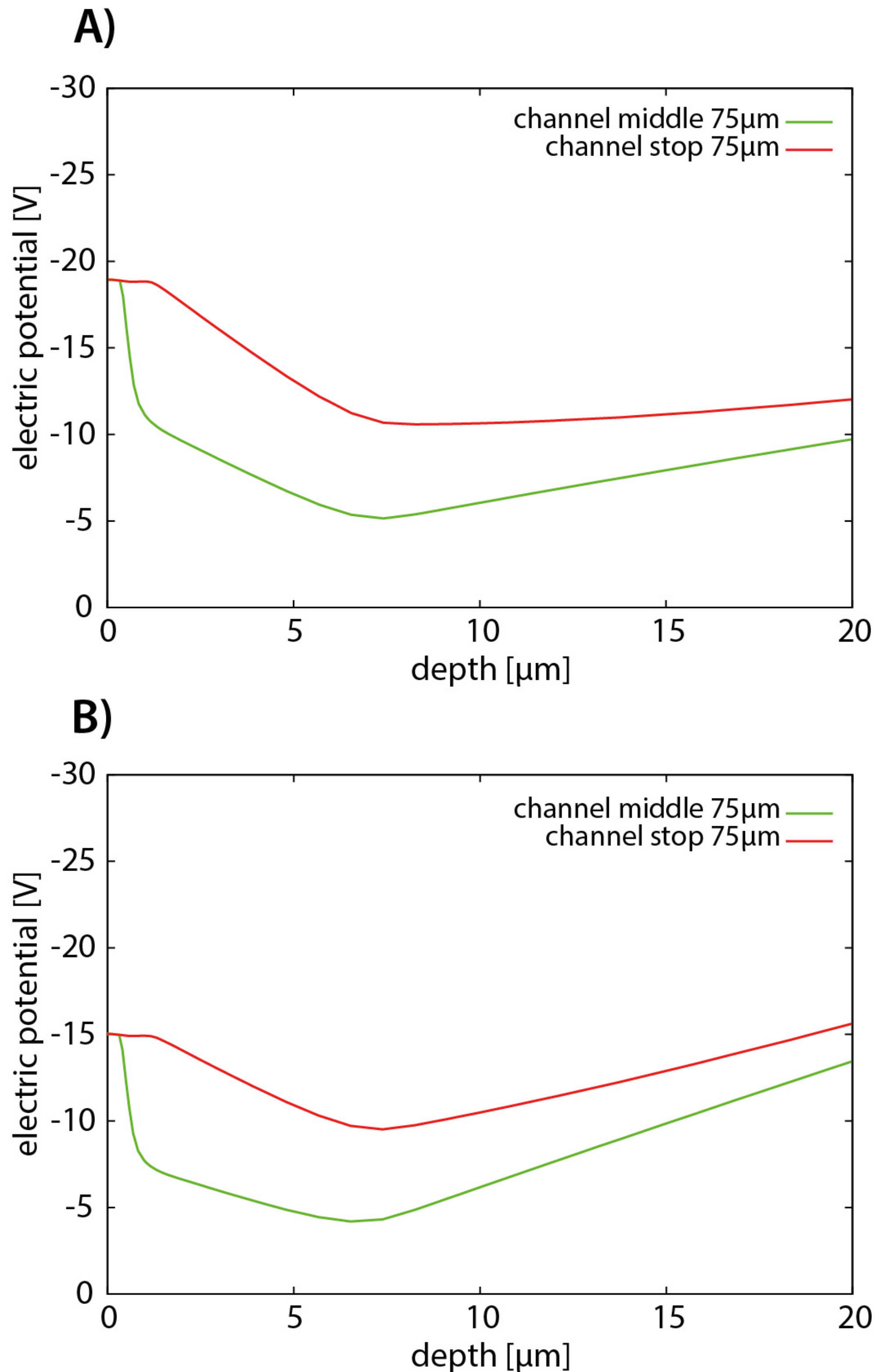

Figure 6.4: Cuts through the electric potential in the row direction for standard operation mode and HCHC-mode. One-dimensional cuts through the electric potential of a two-dimensional simulation in the row direction. The cuts through the middle of the channel notch of the storage register and the channel stop are plotted to a depth of 20 µm. Compared to the standard operation mode (A), a more negative back contact voltage is applied in the high charge handling capacity mode (B). This reduced the difference of the electric potential at a depth of 7 µm and 1.4 µm, so that the electrons can be stored closer to the register side.

6.2 Influence of the operation parameters on the pixel full well capacity

In order to verify that the changes in the electric potential increase the charge handling capacity, signal charges are injected into the center pixel of the simulation region and the charge spilling is observed in dependence of the number of generated electrons. Since the channel stops are the weaker potential barrier, the charge handling capacity was determined from the simulations in the row direction. In the numerical device simulations, a certain number of signal charges can be injected at a certain position in the device. To avoid charge spilling due to the expansion of the charge cloud, the signal charges were injected at a depth of 20 µm below the register side (section 4.3.1). After charge collection, the number of electrons in the center pixel is identified.
Therefore, the simulation tool introduces sub-regions in the grid of the simulated region and sums up all charges in these regions. One pixel corresponds to one sub-region. A pixel is defined as the region between two neighboring channel stops up to a depth of 20 µm below the register side. So, the signal charges are injected in the center pixel and charges in the adjacent pixels reach these pixels only by charge spilling. The charge spilling is defined to start when 95% of the generated signal electrons are inside the center pixel.
The charge handling capacity in standard operation mode used for spectroscopy derived from the simulations is 3×10^5 electrons. By applying the operation conditions for the high charge handling capacity mode, the pixel full well capacity was increased by a factor of six to approximately 1.8×10^6 electrons.
Figure 6.5 shows the electron density distribution for both operation modes. The electron density was plotted for two pixels until a depth of 20 µm in the units of electrons per µm^3. The charge was initially generated at x = 112.5 µm, which is the middle of the center pixel. The pixel border is at 75 µm. In both cases, 2×10^6 electrons were generated.
In figure 6.5A, the standard operation voltages are applied. Since the charge handling capacity in this mode is 3×10^5 electrons, there is a significant charge spilling into the neighboring pixels. The simulations of the electric potential without signal charges showed that the global potential minimum for electrons in standard operation mode is at a depth of 7 µm below the register side. In figure 6.5A, most of the signal charges are stored at a depth of 7 µm. A small fraction of the electrons can overcome the potential barrier to the local potential minimum at a depth of 1.4 µm and are stored closer to the surface.

In the mode for enhanced charge handling capacity shown in figure 6.5B, the charge spilling is significantly reduced. Most of the signal electrons are stored at a depth of 1.4 µm below the register side, which is the depth of the global potential minimum in HCHC-mode. Only a few electrons overcome the potential barrier to the potential minimum at a depth of 7 µm.

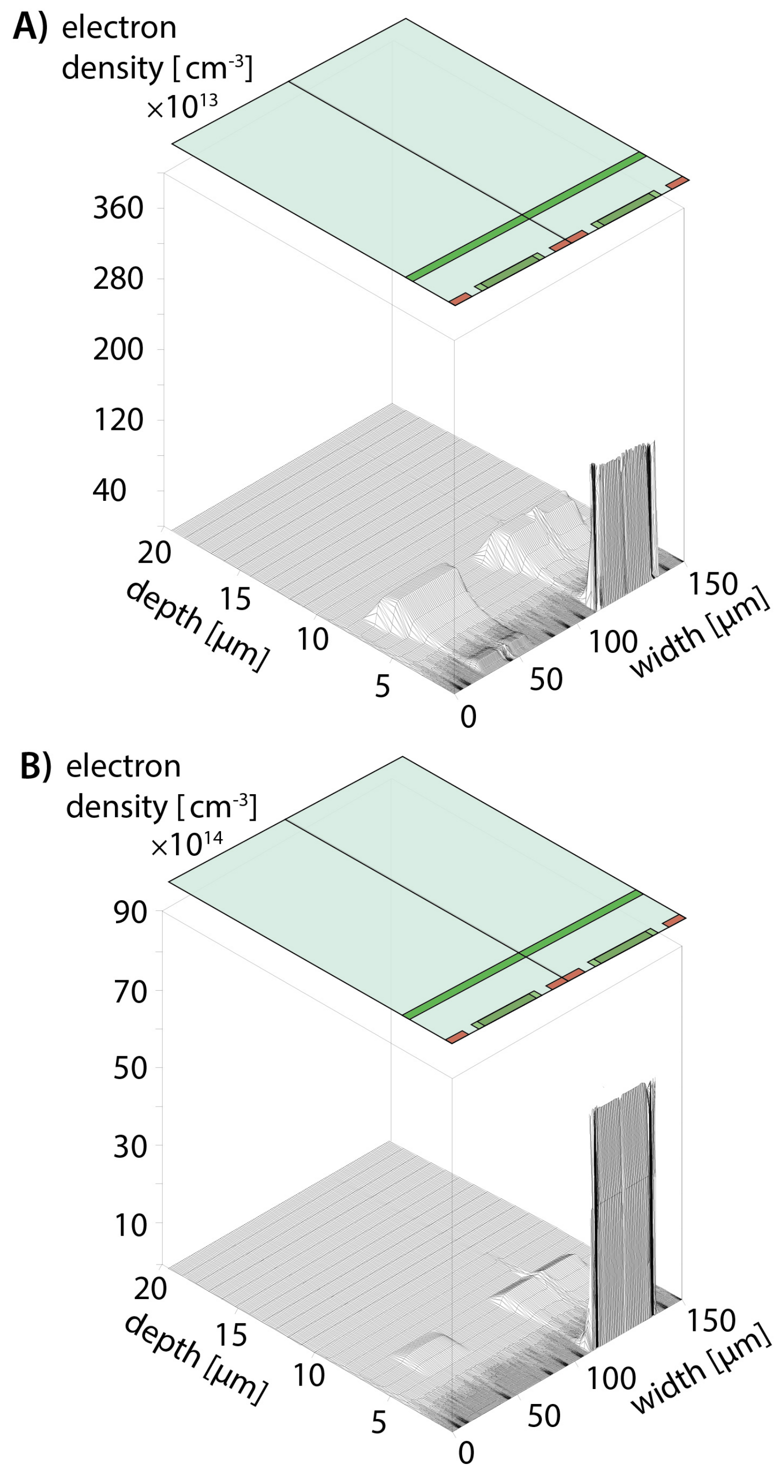

Figure 6.5: Two-dimensional numerical simulations of charge spilling along row direction. The plots show the charge density distribution of 2×10^6 electrons in the units of electrons per μm^3. The charges were generated at a depth of 20 µm below the register side at a lateral position of x = 112.5 µm. The pixel border is at 75 µm. A) Electron density distribution in standard operation mode used for spectroscopy. B) Electron density distribution in HCHC-mode. The storage depth is shifted closer to the register side and the charge spilling into adjacent pixels is reduced compared the standard operation mode.

6.3 Effect of the space charge distribution

The space charge distribution inside the device also has an influence on the electric potential of the pixel structure and will be studied in the following sections. One has to distinguish between fixed space charges and mobile charge carriers in the device. Fixed space charges of dopants are inserted in the device during the production process at a distinct location by ion implantations or as part of the doping of the silicon bulk material. Mobile charge carriers are generated during the operation of the detector in the form of signal charges or for example thermally generated electrons and holes. In both cases, the presence of charges affects the electric potential of the pnCCD according to equation (6.1).

6.3.1 Influence of fixed space charges

In section 6.1, the pixel full well capacity was increased by increasing the potential barrier between neighboring pixels and by shifting the storage depth of the electrons closer to the surface with the appropriate operation voltages. In order to achieve a further improvement of the charge handling capacity, the potential barrier has to be further increased and the potential minimum for electrons has to be shifted closer to the register side. This can be achieved by changing the electric potential with fixed space charges. Therefore, the ion implantation process parameters of the pixel structure implants and the doping of the silicon bulk material were optimized for enhanced charge handling capacity.
As already mentioned in section 3.2.1, the pixel structure of the pnCCD consists of different n- and p-implants. The positive space charges of the depleted n-implants of channel notch and channel guide attract electrons and form a local potential minimum, where the signal electrons are stored. The negative space charges of the depleted p-implant channel stops repulse electrons and therefore form a local potential maximum for electrons, which acts as potential barrier between neighboring pixels. An increase in the implantation dose of the n-doped channel notch and channel guide region makes this domain more attractive for electrons. An increase of the channel stop p-implantation dose makes this region more repulsive for electrons, as there are more negative space charges in these areas. Both changes increase the pixel full well capacity, as they increase the potential barriers between the pixels, especially in the row direction, the predominant spilling direction.
Increasing the implantation doses of those two regions can also lead to an increase of leakage current between the implantation areas of the p^+-registers and the channel

notch and channel guide. The increased electric field results in so-called “bright pixels” or “noisy pixels”, which are pixels with thermally generated currents. The increase of the implantation doses can degrade the other pnCCD properties, such as noise or the CTE. The electric field generated by the fixed space charge regions must therefore be limited by the electric field strength in silicon to avoid breakdown. The height of the potential barrier between the pixels in the row direction is mainly determined by the absence of n-implants between the neighboring pixels.
Another possibility to increase the charge handling capacity is to shift the storage depth of the signal electrons closer to the register side. If the difference between the electric potential of the register side and the back contact is held constant, the storage depth decreases by decreasing the bulk-doping of the silicon substrate. The doping of the silicon wafer determines its resistivity and thus its depletion voltage. A decrease in the bulk-doping results in an increase of the resistivity of the material and a decrease of the depletion voltage. The pnCCDs are operated fully depleted, respectively overdepleted to fix the potential minimum at a depth of 7 µm below the register side. Any further enhancement of the back contact voltage beyond the depletion voltage leads to a shift of the potential minimum closer to the register side.
Figure 6.6 shows one-dimensional cuts through the two-dimensional simulation in the channel direction for two different CCDs. CCD 1 has lower implantation doses of the pixel implantations and a higher bulk doping of the silicon substrate compared to CCD 2 and therefore corresponds to the CCD simulated in the previous chapters. In CCD 2, the implantation doses of the pixel implants are increased and the bulk doping of the silicon substrate is decreased according to our considerations.
At a given potential difference between the potential at the register side and the back contact, the potential minimum at a depth of 1.4 µm is more pronounced in case of high-resistivity silicon as used in CCD 2 (figure 6.6). The gradient of the electric potential from the register side to the back contact is much steeper due to lower bulk doping. The global potential minimum can be shifted from a depth of 7 µm to a depth of 1.4 µm with a smaller difference between the potential at the register side and the back contact by using silicon with a higher resistivity.
By adjusting the space charge distributions and the operation conditions in our simulations according to our considerations, the pixel full well capacity was increased to approximately 2.8×10^6 electrons in CCD 2 compared to 1.8×10^6 electrons in high charge handling capacity mode in CCD 1. This corresponds to about 10^4 X-ray photons with an energy of 1 keV.

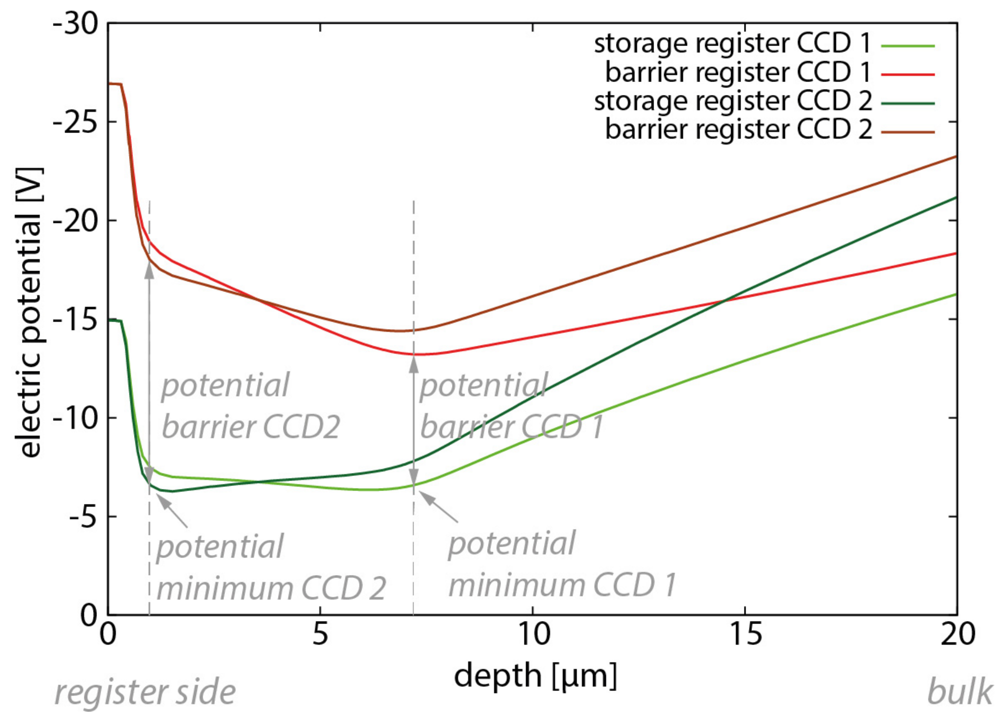

Figure 6.6: Electric potential in the channel direction for different space charge distributions. If the space charge distribution is optimized for a high charge handling capacity as in CCD 2, the potential minimum of the signal electrons is shifted closer to the register side and the potential barrier is increased. This is achieved by using silicon with a higher resistivity and by increasing the ion implantation dose of the n-implant channel notch and channel guides compared to CCD 1. In both simulations, the identical operation parameters for the high charge handling capacity mode are applied.

6.3.2 Influence of mobile charge carriers

The electric potential inside the pnCCD is formed by the applied operation voltages and the fixed space charges of the n- and p-implants as well as the bulk doping. Mobile charge carriers, for example, the signal electrons, influence the electric potential in their surrounding region, too. Their effect on the electric potential of a certain region in the detector increases with the number of charge carriers. If very high amounts of signal electrons are stored in one pixel, the negative charge of the signal electrons shifts the electric potential of this area to more negative values. The signal electrons therefore have an influence on the potential well in which they are stored (equation (6.1)).
Figure 6.7 shows cuts through the electric potential in the row direction for different amounts of signal electrons. The simulations were performed for the operation voltages for the enhanced charge handling capacity mode. Different amounts of signal electrons, ranging from no electrons to 9×10^5 signal electrons were injected into the center pixel. Since the maximum number of injected electrons is smaller than the charge handling capacity in HCHC-mode, there is no charge spilling into neighboring pixels. The simulation was performed in the row direction through the middle of a storage register. The one-dimensional cuts were performed through the electric potential of the center pixel (figure 6.7A), an adjacent channel stop (figure 6.7B) and the channel notch of an adjacent pixel (figure 6.7C). If there are no signal electrons injected into the device, there is a global potential minimum at a depth of 7 µm and a local potential minimum at a depth of 1.4 µm. Since the influence of the barrier registers and MOS contacts is not simulated, the potential minimum is at a depth of 7 µm for the operation voltages used in HCHC-mode. The electrons are therefore stored at a depth of 7 µm (figure 6.8A). The negative charge of the signal electrons shifts the potential minimum in this depth to more negative values until it is on an equipotential line with the potential at a depth of 1.4 µm. Now the electrons are also stored at a depth of 1.4 µm (figure 6.8B). Their negative charges shift the electric potential in this depth to more negative values, and more electrons are stored closer to the register side (figure 6.8C). The electric potential under the adjacent pixel and channel stop is almost unaffected.

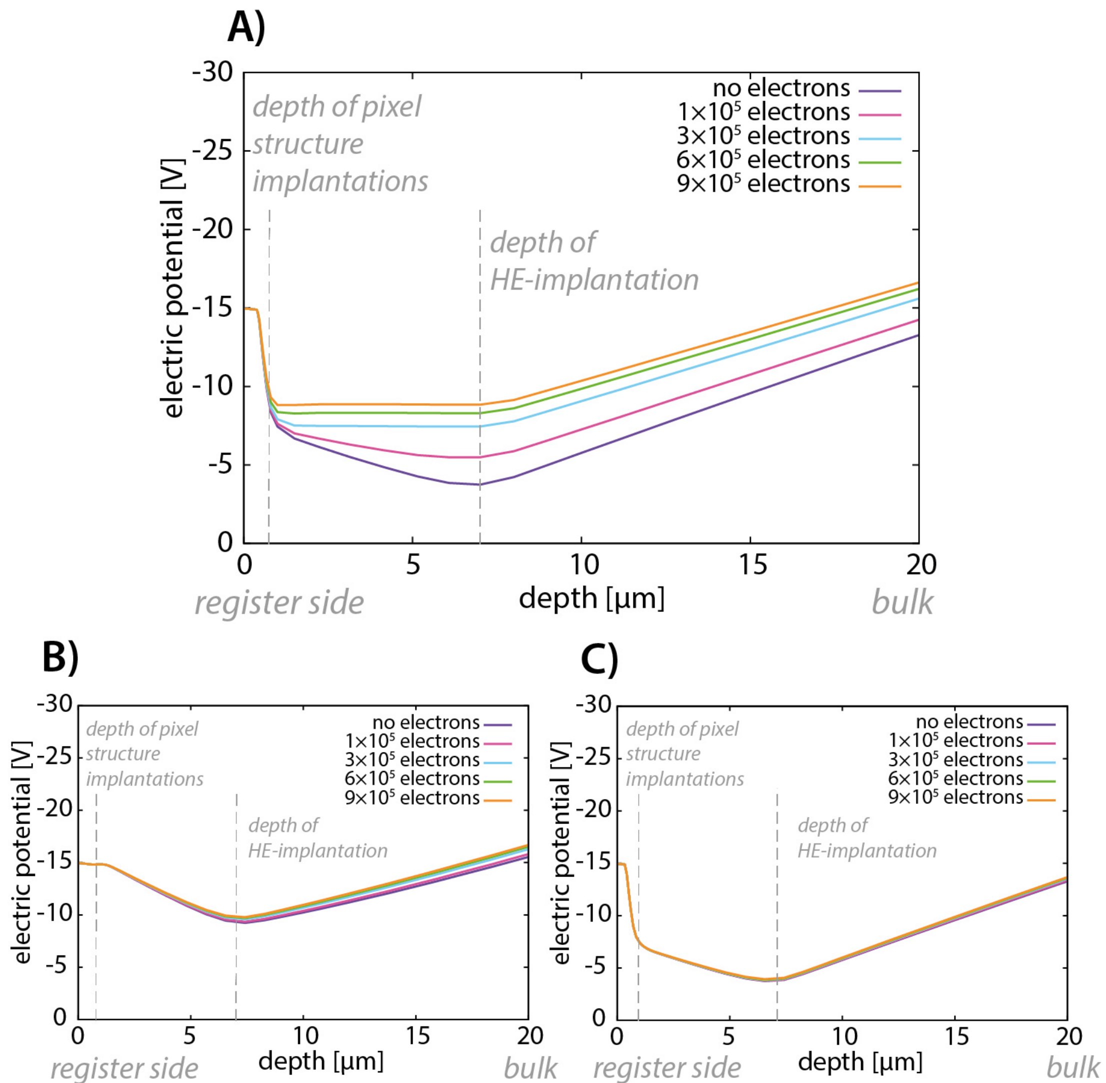

Figure 6.7: One-dimensional cuts through the electric potential in the row direction for different amounts of charges stored in the center pixel. The operation parameters for the high charge handling capacity mode are applied. A) Cut through the middle of the pixel in which the electrons are stored. B) Cut through the adjacent channel stop. C) Cut through the neighboring pixel. There is no charge spilling into the neighboring pixels. The negatively charged signal electrons shift the electric potential of their storage location to more negative values. With increasing numbers of electrons, the potential minimum at a depth of 7 µm is shifted to more negative values until it is on a equipotential line with the electric potential at a depth of 1.4 µm. The electric potential below the channel stop and the adjacent pixel is almost not affected.

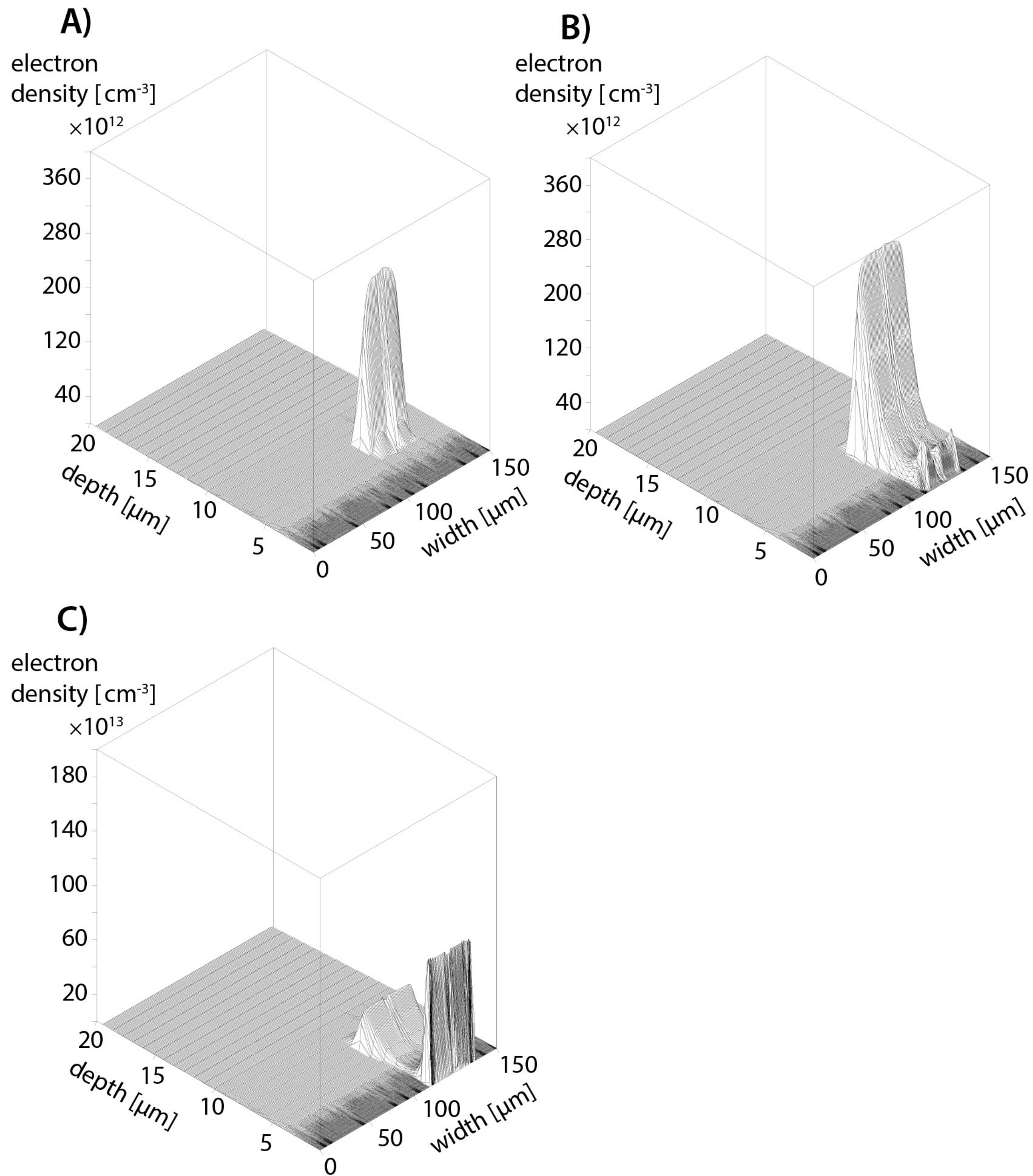

Figure 6.8: Simulation in the row direction of the charge density distribution of different amounts of signal charges. The operation voltages for the high charge handling capacity mode are applied and are therefore identical for all simulations. 1×10^5 electrons (A), 3×10^5 electrons (B) and 6×10^5 electrons (C) were generated in the pnCCD. With increasing numbers of electrons, the storage depth is shifted closer to the register side. The reason is the influence of the negatively charged electrons on the electric potential in their vicinity.

6.3.3 Dependence on the pixel geometry

Besides the height of the potential barrier and the storage depth, the area in which the signal electrons are stored is also an important factor that influences the pixel full well capacity (section 6.1). The electrons are not stored under the whole pixel area, rather in the area of the channel notch and channel guide implants. During a three-phase transfer, the whole amount of signal electrons is located under only one p^+-register at a point in time. Therefore, the charge handling capacity of a pnCCD corresponds to the number of electrons that can be stored under one channel notch respectively channel guide.
In order to study the effect of the storage area, pnCCDs with different pixel sizes were used. The charge handling capacity of pnCCDs with a pixel size of 75 µm × 75 µm is compared to those with a pixel size of 48 µm × 48 µm. For these pnCCDs, the area of the channel notch and channel guide implantations do not scale with the pixel size. Although, the pixel size of the 75 µm pnCCDs is approximately only two and a half times larger than the size of the 48 µm pixels, the area of the channel guide differs by a factor of four and the area of the channel notches almost by a factor of nine. The reason is that the pixel layout of the pnCCDs with a pixel size of 48 µm × 48 µm was optimized for high-resolution spectroscopy experiments. In those experiments, the number of signal electrons is low and therefore can be completely stored under the channel notch. If the area under which the signal electrons are stored is small, the signal charges are shifted over fewer defects in the silicon during their transfer to the readout anode as if the storage area would be larger. The charge transfer efficiency increases, which improves the spectroscopic performance of the pnCCD. Increasing the area under which the signal charges are stored, increases the charge handling capacity, but also the number of defects (electron traps) over which the signal charges are transferred. For high amounts of signal charge of several 10^5 electrons per pixel per frame, the loss of a few electrons due to electron traps is negligible.
Figure 6.9 shows cuts through the electric potential in the channel and in the row direction for both 75 µm and 48 µm pnCCDs in standard operation mode used for spectroscopy. For both cuts, the potential barrier to the neighboring pixels is higher for pnCCDs with a pixel size of 75 µm × 75 µm. So, the different pixel geometries have an influence on the electric potential in the bulk. The relative areas of the channel notch and channel guide is smaller for 48 µm pnCCDs compared to the rest of the pixel size. Specially, the dimension of the channel notch in the row direction is much smaller for 48 µm pnCCDs than for 75 µm pnCCDs. The dimension of the channel stops almost scales with the pixel size. In figure 6.9A and figure 6.10A, cuts through the electric

potential in the row direction for both pixel sizes are plotted for the standard operation mode and the HCHC-mode.

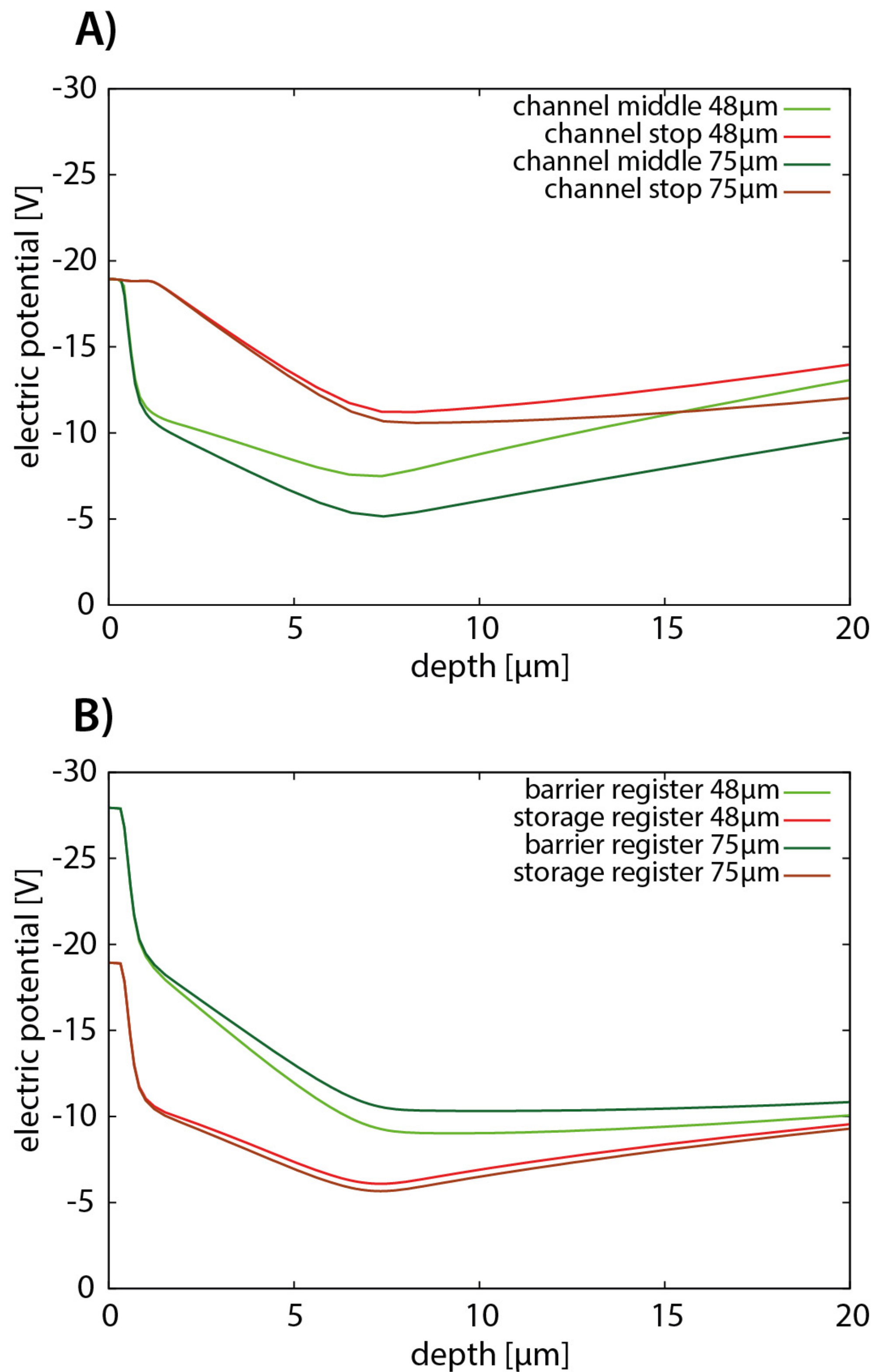

Figure 6.9: Simulation of the electric potential for pnCCDs with different pixel sizes in standard operation mode. Depicted are one-dimensional cuts in A) the row direction and B) the channel direction up to a depth of 20 µm below the register side. The pixel sizes are 48 µm × 48 µm and 75 µm × 75 µm. The operation parameters for the standard operation mode are used.

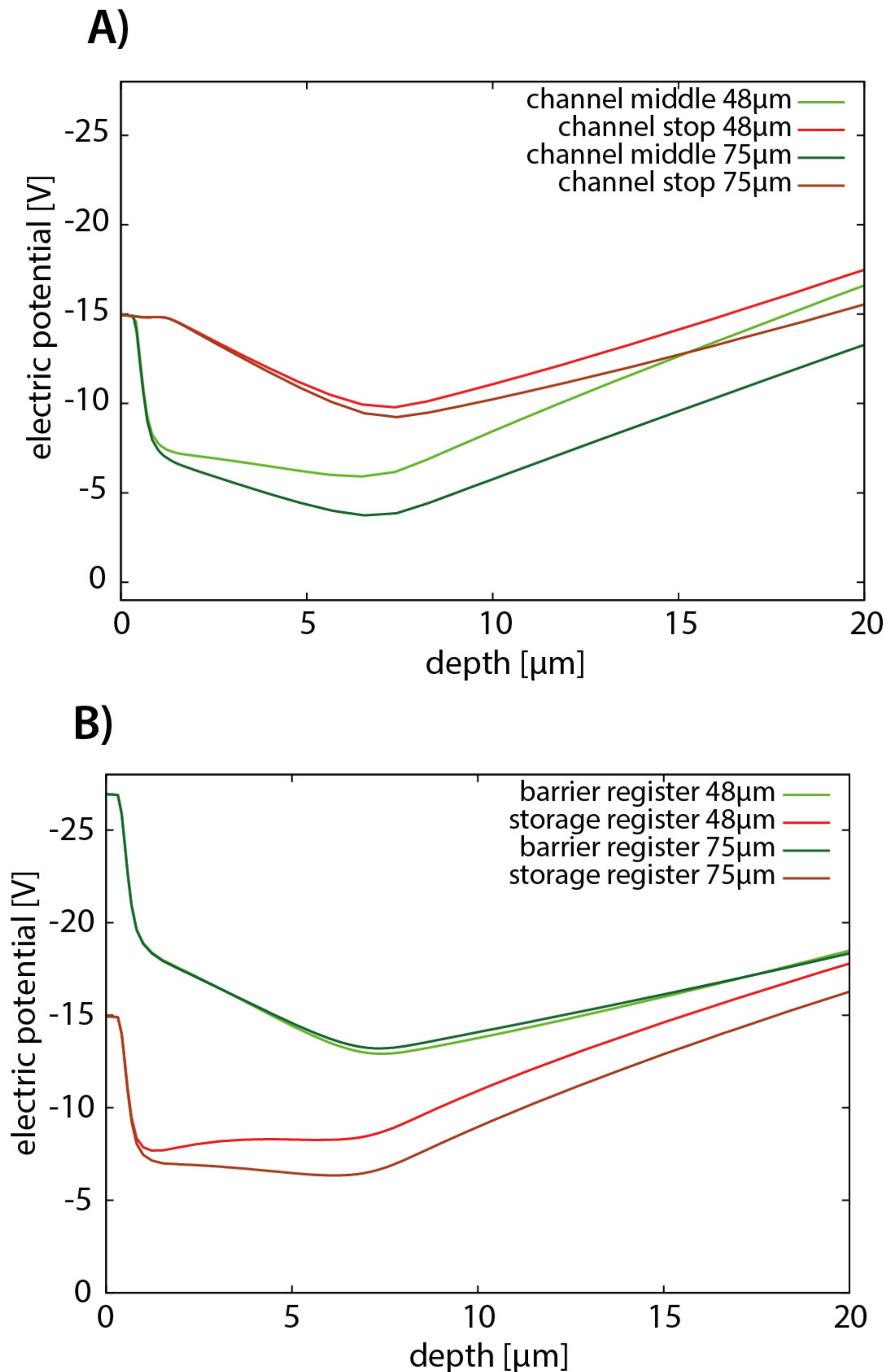

Figure 6.10: Simulation of the electric potential for pnCCDs with different pixel sizes in HCHC-mode. The plots show one-dimensional cuts for A) simulation in the row direction and B) simulation in the channel direction up to a depth of 20 µm below the register side. The pnCCDs have pixel sizes of 48 µm × 48 µm and 75 µm × 75 µm. The operation voltages for the enhanced charge handling capacity mode are used.

As shown in section 5.2, for the simulation in the row direction, the third dimension, which is the dimension of the register contact in the channel direction, is not taken into account, since the third dimension is assumed to be constant and the register contact extends over the whole register side. The electric potential of the areas of the channel notch, channel guide and channel stop interact. Since the area of the n-implants of the channel notch is much smaller for the 48 µm pnCCDs, their positive space charges have less influence on the electric potential than the applied negative voltage. Therefore, the electric potential under the channel notch is more negative and the difference between the global potential minimum at a depth of 7 µm and the electric potential at a depth of 1.4 µm is smaller for pnCCDs with a pixel size of 48 µm × 48 µm. More signal electrons can overcome the potential barrier between the two potential regions and are stored closer to the register side for 48 µm pnCCDs. There is only a slight difference in the electric potential of the channel stops. In the channel direction (figure 6.9B and figure 6.10B), the dimension of the aluminum contacts is taken into account. The differences in the dimension of the channel notches are smaller than in the row direction. Therefore, the differences in the electric potential under the channel notches are also smaller. The negative back contact voltage has a stronger influence on the electric potential, if the pixel size is smaller. The reason is that the separation depth, which is the depth were the signal electrons are separated into the different pixels, is approximately the pixel size [29]. From the surface of the register side to the separation depth, the influence of the register side on the electric potential is dominant. If the pixel size is smaller, the influence of the back contact on the electric potential is more pronounced. If the same back contact voltage is applied in high charge handling capacity mode, the storage depth of the electrons is shifted closer to the register side for 48 µm pnCCDs than for 75 µm pnCCDs (figure 6.10B).
The electric potential of both 48 µm and 75 µm pnCCDs is plotted as equipotential lines in figure 6.11 for simulations in the row direction. The smaller dimension of the channel notch implants compared to the channel guide implants of the 48 µm pnCCDs becomes apparent in the distribution of the electric potential.

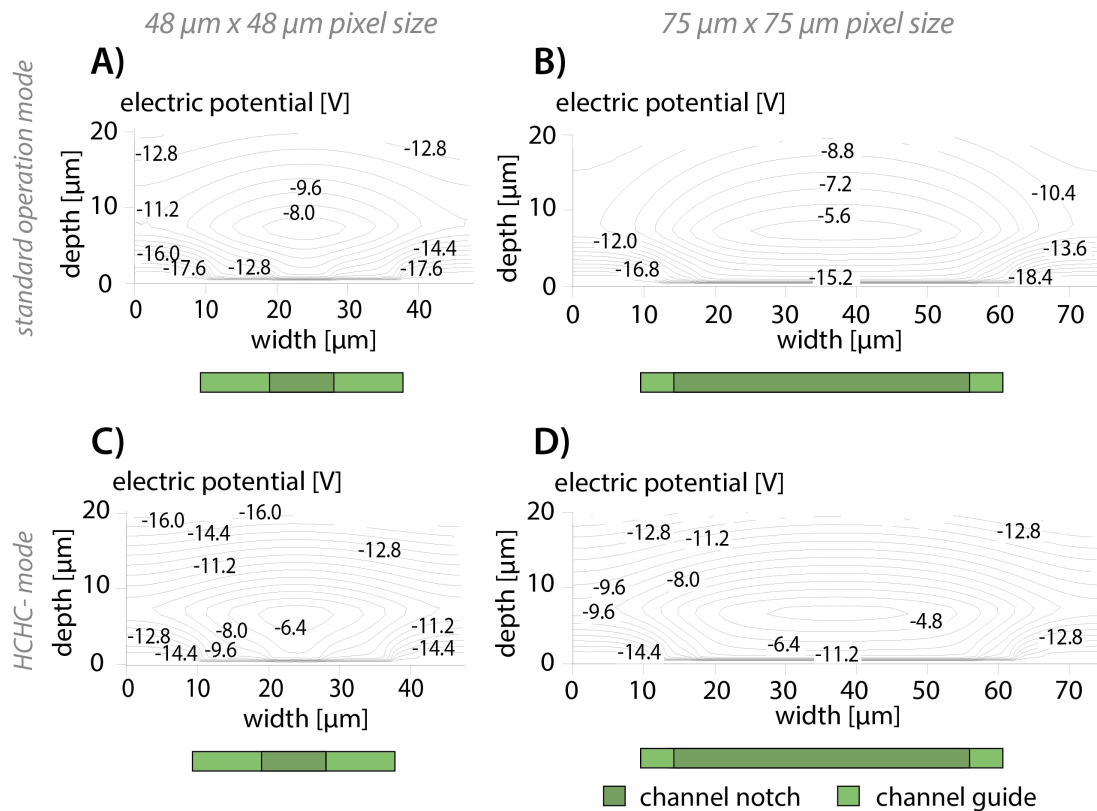

Figure 6.11: Equipotential isolines of the pnCCD pixels. The electric potential in the row direction was simulated for 48 µm and 75 µm pnCCDs up to a depth of 20 µm. In A) and B), the operation parameters for the standard operation mode are used whereas in C) and D) the operation parameters for the HCHC-mode are applied. The regions of the channel notch and channel guide implants project in the electric potential.

This influences the distribution of the signal electrons in this area (figure 6.12). In HCHC-mode, the signal charges are mainly stored in the global potential minimum at a depth of 1.4 µm (figure 6.10). At this depth, the electrons accumulate predominantly in the region of the channel notches. Electrons, which are stored deeper in the bulk at a depth of 7 µm, increasingly accumulate under the channel guides (figure 6.12A). From the simulations, a charge handling capacity of 6×10^4 electrons in standard operation mode and 3×10^5 electrons in HCHC-mode is obtained for 48 µm pnCCDs. For pnCCDs with a pixel size of 75 µm × 75 µm having comparable n- and p-implantation doses and bulk doping, as well as operation voltages, the pixel full well capacity is 3×10^5 electrons in standard operation mode and 1.8×10^6 electrons in HCHC-mode. In both operation modes, the pixel full well capacities of 48 µm and 75 µm pnCCDs differ by a factor of approximately five to six. According to the model that relates the charge handling

capacity to an electric capacitance, the number of stored electrons is proportional to the storage area (section 11). The signal charges are preferably stored under the area of the channel notch. For high numbers of signal electrons, the charges are also stored under the channel guide (figure 6.12B). If the number of signal electrons exceeds the pixel full well capacity, the charges start to spill over the potential barrier in the row direction. While the adjacent pixels are filled with signal electrons, the region of the channel guide implants becomes more attractive for electrons. The signal electrons are now also stored in the region of the channel guides and the number of electrons stored in the center pixel increases, although the excess charges are spilling into the neighboring pixels. The area of the channel guide of the 75 µm pnCCDs is four times larger than the area of the 48 µm pnCCDs. The areas of the channel notches differ by a factor of nine. The charge handling capacity therefore scales with the size of the storage area. The electrons are preferentially stored under the channel notch implants. With increasing number of electrons, they are also stored under the channel guides. Since the difference between the area of channel notch and channel guide is less in pnCCDs with a pixel size of 75 µm × 75 µm than for a pixel size of 48 µm × 48 µm, this effect is less pronounced for 75 µm pnCCDs.

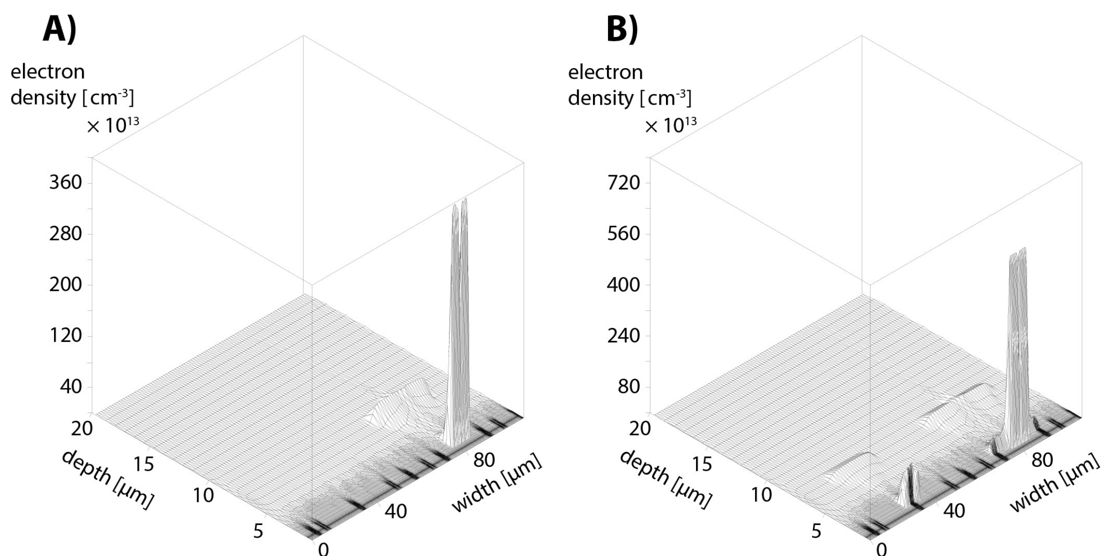

Figure 6.12: Simulation of the electron density distribution of a 48 µm pnCCD in the row direction for HCHC-mode. A) If the amount of signal electrons is below the pixel full well capacity, the charges are mainly stored in the region of the channel notch implants. Electrons that are stored deeper in the substrate, are also located in the area of the channel guides. B) If the number of signal electrons exceeds the pixel full well capacity, the charges start to spill over the potential barrier in the row direction and the region of the channel guides becomes more attractive for electrons.

Summary of chapter 6

The influence of the operation voltages, space charge distribution and pixel geometry on the electric potential and the pixel full well capacity was presented. In principle, there are three parameters that affect the charge handling capacity: the height of the potential barrier to the neighboring pixel and according to the model, in which the charge handling capacity is compared to the electric capacitance of a parallel-plate capacitor, the storage depth underneath the register side and the dimension of the area under which the signal electrons are stored. The simulation showed that by optimizing the operation voltages and the space charge distribution of the pnCCD, the pixel full well capacity can be increased from 3×10^5 electrons in standard operation mode to 2.8×10^6 electrons in high charge handling capacity mode using a pnCCD with enhanced ion implantation process parameters of the pixel structure and a higher resistivity of the silicon bulk material. Furthermore, it was shown that the charge handling capacity scales with the area of the channel notch implants under which the signal electrons are stored.

7 Electric potential profile during charge transfer

In a pnCCD, the signal charges are transferred anlong the channel by a three-phase transfer. The register voltages are periodically changed, so that the signal electrons are alternately stored under one or two transfer registers (figure 3.2). Since during the transfer of signal charges both states have to be passed through, it is irrelevant for the measured charge handling capacity whether the signal charges are stored under one or two registers during integration time. The pixel full well capacity is limited by the state with the lowest charge handling capacity, which is the state in which the signal charges are stored under one register. The simulation showed, that for storage under one register, approximately 2.8×10^6 electrons can be stored in one pixel, whereas for storage under two registers, approximately 3×10^6 electrons can be stored in the high charge handling capacity mode.
Figure 7.1 and figure 7.2 illustrate the differences in the electric potential for storage under one and two registers in HCHC-mode for simulation in the channel direction. Figure 7.2A shows cuts through the middle of the transfer registers for storage under one and two registers and figure 7.2B shows cuts through the corresponding MOS contacts. The electric potential was simulated without the presence of signal charges. If the electrons are stored under one register, this means that, at one of the three registers in a pixel, the Φ-offset voltage is applied, whereas at the other two registers the Φ-offset and Φ-amplitude voltages are applied (section 5.1). The potential barrier between the storage and the barrier register is comparable in both states. For storage under one register, the potential minimum at a depth of 7 µm has a more negative value. This enables the signal electrons to be stored closer to the register side, since the difference between the electric potential at a depth of 7 µm and 1.4 µm is reduced compared to the state where the signal electrons are stored unter two registers. At a depth of 1.4 µm, the potential barrier between storage and barrier register is higher than at a depth of 7 µm.

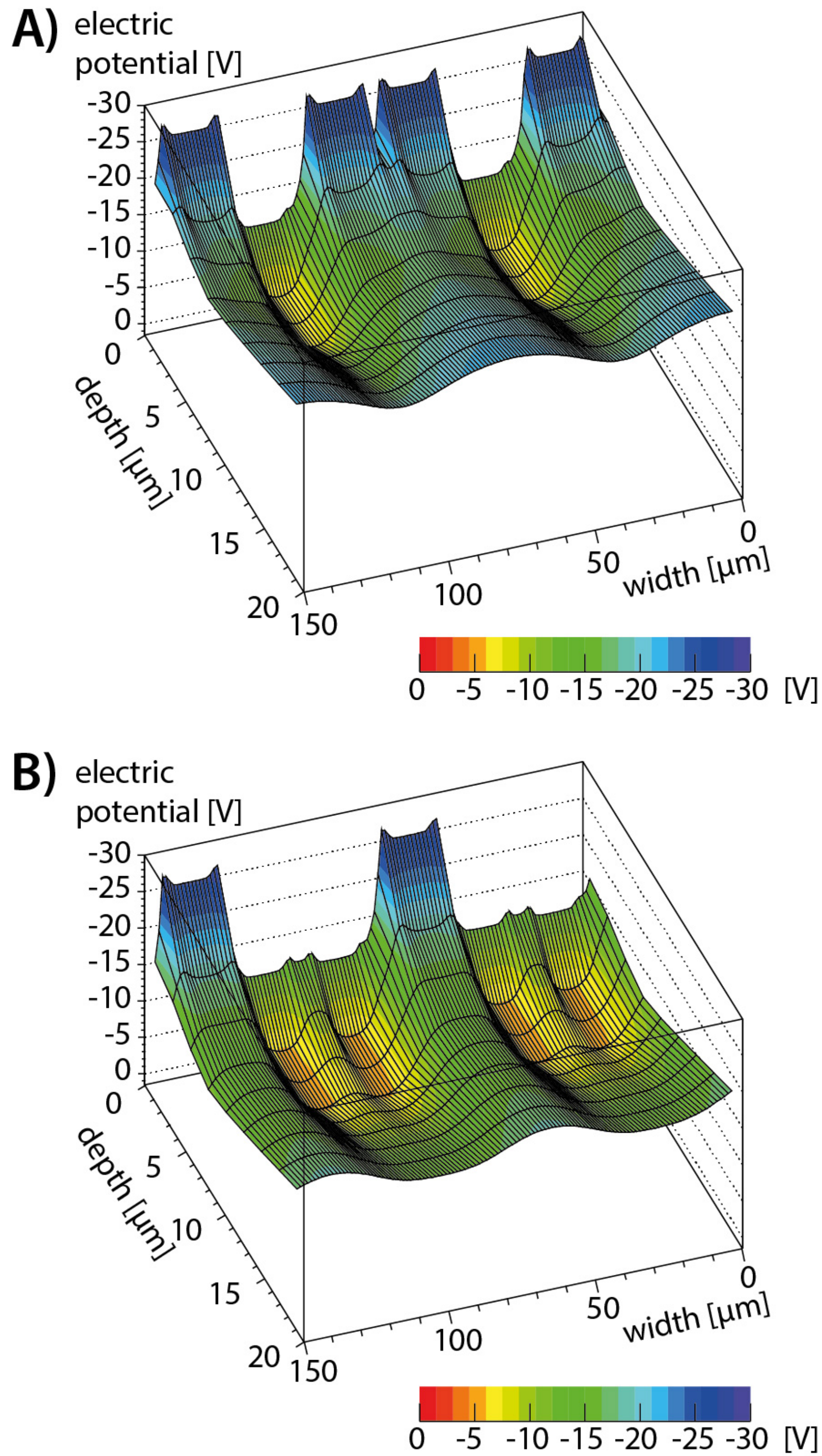

Figure 7.1: Electric potential for one and two register storage. The electric potential is simulated without the presence of signal electrons. A) Simulation in the channel direction for storage under one register. B) Simulation in the channel direction for storage under two registers. The electric potential for storage under one register is more pronounced than for storage under two registers.

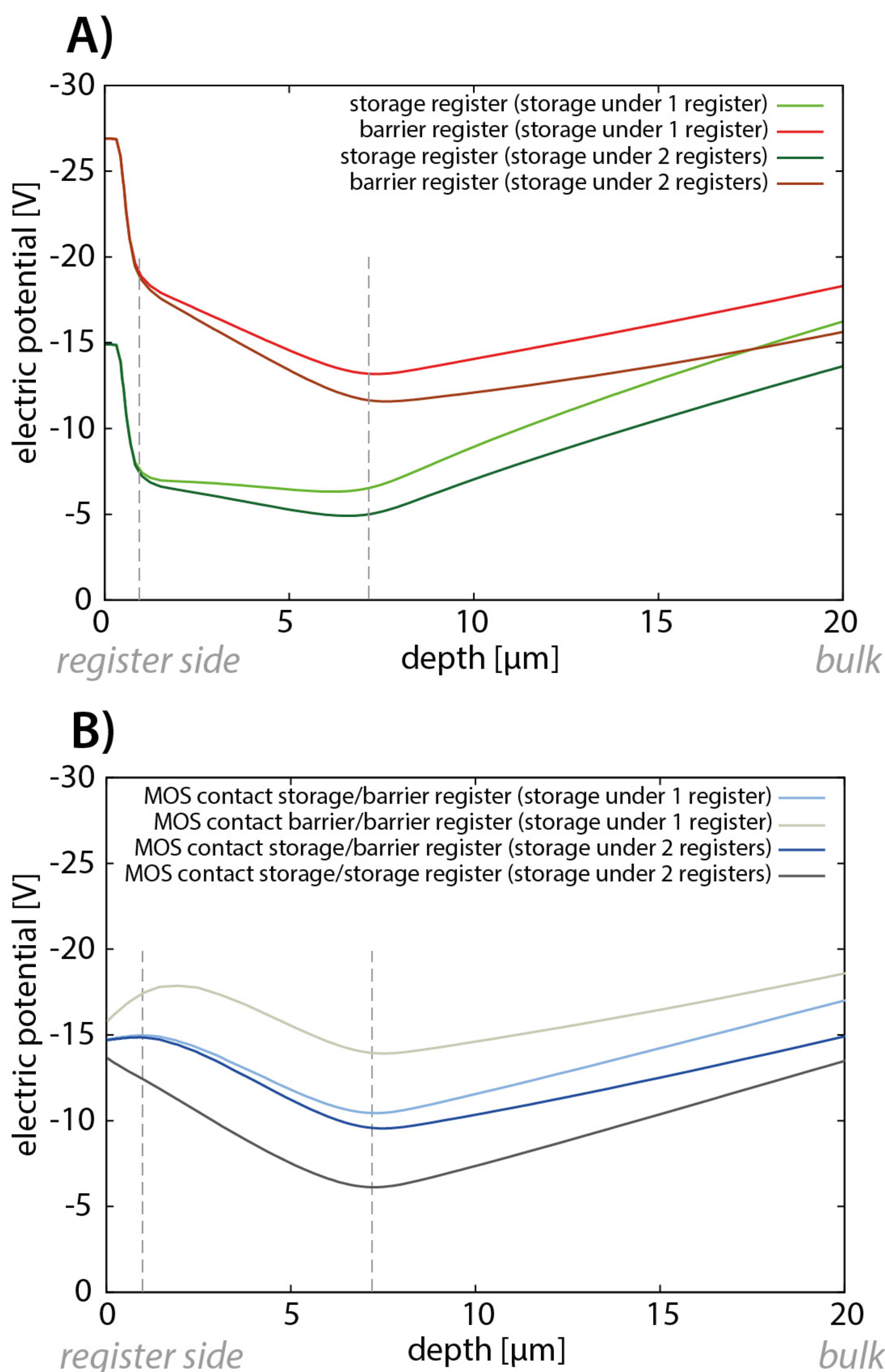

Figure 7.2: One-dimensional cuts through the electric potential in the channel direction for storage under one and two registers. During the charge transfer to the readout anode, the charges are alternately stored under one and two registers. A) Cuts through the storage and barrier register from the register side to a depth of 1.4 µm. B) Cuts through the MOS contacts. If the signal charges are stored under one register, they are located closer to the register side as the potential minimum is shifted closer to the register side from a depth of 7 µm to a depth of 1.4 µm.

Summary of chapter 7

During the transfer of the signal charges along the channel, the electrons are alternately stored under one and two registers, independent of the state during integration time. The state with the smallest charge handling capacity during transfer defines the maximum pixel full well capacity. Since for storage under one register fewer electrons can be stored in one pixel than for storage under two registers, the maximum amount of signal electrons that can be stored under one register determines the charge handling capacity of the pnCCD pixels.

8 Controlled charge extraction

In the high charge handling capacity mode, the pixel full well capacity was increased up to 2.8×10^6 signal electrons, corresponding to approximately 10^4 X-ray photons with an energy of 1 keV. However, since the number of X-rays in the primary beam of an FEL can be as high as 10^{13} X-rays per pulse with a duration of less than 100 fs and the X-rays in a single Bragg reflection can exceed 10^7 photons, blooming effects can occur even in HCHC-mode.

A common method to prevent charge blooming in conventional CCDs is the so-called antiblooming concept. It is based on the localized and controlled charge removal from the sensor device, usually by the insertion of antiblooming gates [11]. With antiblooming mechanisms, the spatial resolution of the incoming photons can be preserved, but the intensity information is lost in the overflowing pixels. For some imaging experiments, relying on a precise image structure, the preservation of the spatial resolution at the expense of precise intensity information is a workable compromise. In contrast to insulated gate CCDs, notably MOSCCDs, the potential wells of the pixel array of a pnCCD are created by p^+n-junctions, allowing direct electric access to the pixel struture. This allows to directly drain off charges from the pixels and to define a drain level by applying the appropriate operation voltages.

8.1 Antiblooming methods in conventional CCDs

So far, one had to decide between antiblooming or non-antiblooming sensors, as the antiblooming feature was built into the chip. Conventional antiblooming sensors prevent high photon intensity artifacts, but due to their architecture, they struggle with nonlinearity and reduced sensitivity [34]. Depending on the detector design and fabrication technology, different antiblooming methods are used:

- The most common method is the lateral or horizontal antiblooming [9], [35]. Here, the charge spilling into adjacent pixels is avoided by so-called antiblooming gates or implantations [36]. An antiblooming gate electrode (figure 8.1A) or

implantation (figure 8.1B), which drains excess charges from saturated pixels in a controlled manner, is implemented beside each pixel. Instead of spilling over to adjacent pixels, the charges are spilling preferentially over the lowest potential barrier into the antiblooming drain. The lateral overflow drain or horizontal antiblooming structure is easily adjustable by the external voltages applied on the antibloomig gate (V_{ABG}) and drain (V_{ABD}).
The drawback is that the antiblooming structure occupies up to 30% of the pixel structure and thus reduces the detector fill factor and its sensitivity. The areas of the CCD occupied by the antiblooming gates generate a gap between the pixels in one dimension, which reduces the effective resolution of the sensor. Normally, the charge drain starts when the pixels are saturated to approximately 50% inducing a non-linear detector response above a certain charge level [34].

- In vertical antiblooming, the charge drain is located underneath the pixels featuring a compact design (figure 8.1C). In contrast to horizontal antiblooming, it does not require light sensitive space on the detector. Because of the complex structure, these CCDs are difficult to optimize and the effective penetration depth for radiation decreases, reducing the detector sensitivity in the red and infrared [9].

- The clocked or charge pumped antiblooming mechanism gives electrons the opportunity to recombine with holes before they spill over into adjacent pixels (figure 8.2). The holes, which are necessary for recombination, are stored in the interface states of the MOS shift registers. It is important to provide a sufficient amount of holes, so that they can effectively recombine with the excess signal electrons before blooming occurs. Using this mechanism, no light-sensitive area is occupied, but a complicated clocking scheme is needed. Since all CCD processing technologies are optimized to keep the number of interfaces states as low as possible, it is difficult to supply enough interface states for recombination [9].

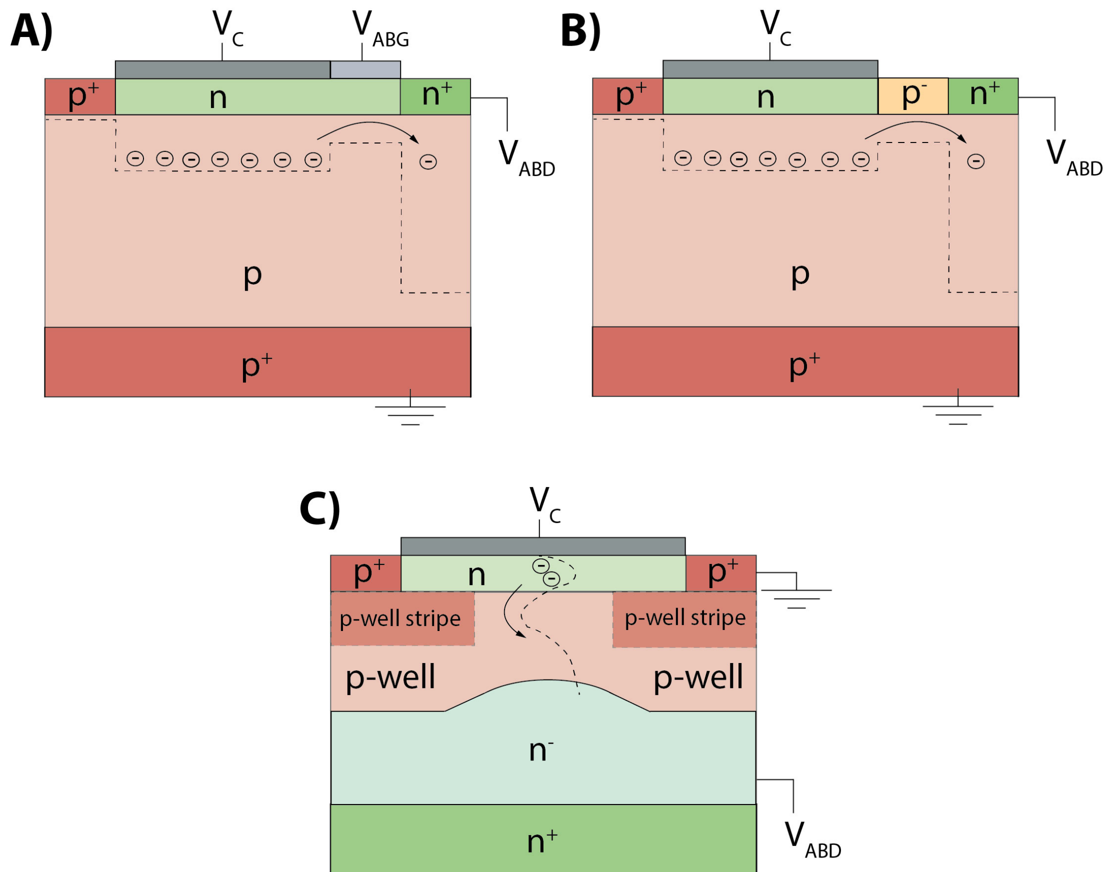

Figure 8.1: Antiblooming structures in conventional CCDs. In conventional CCDs, the antiblooming structures are built in the pixel structure. Cuts through the pixel structure in the transfer direction are depicted. In lateral antiblooming CCDs, additional antiblooming gates (A) or implantations (B) are implemented in the CCD. In vertical antiblooming devices (C), a reversed-biased junction underneath the pixel is used to siphon off excess charges.

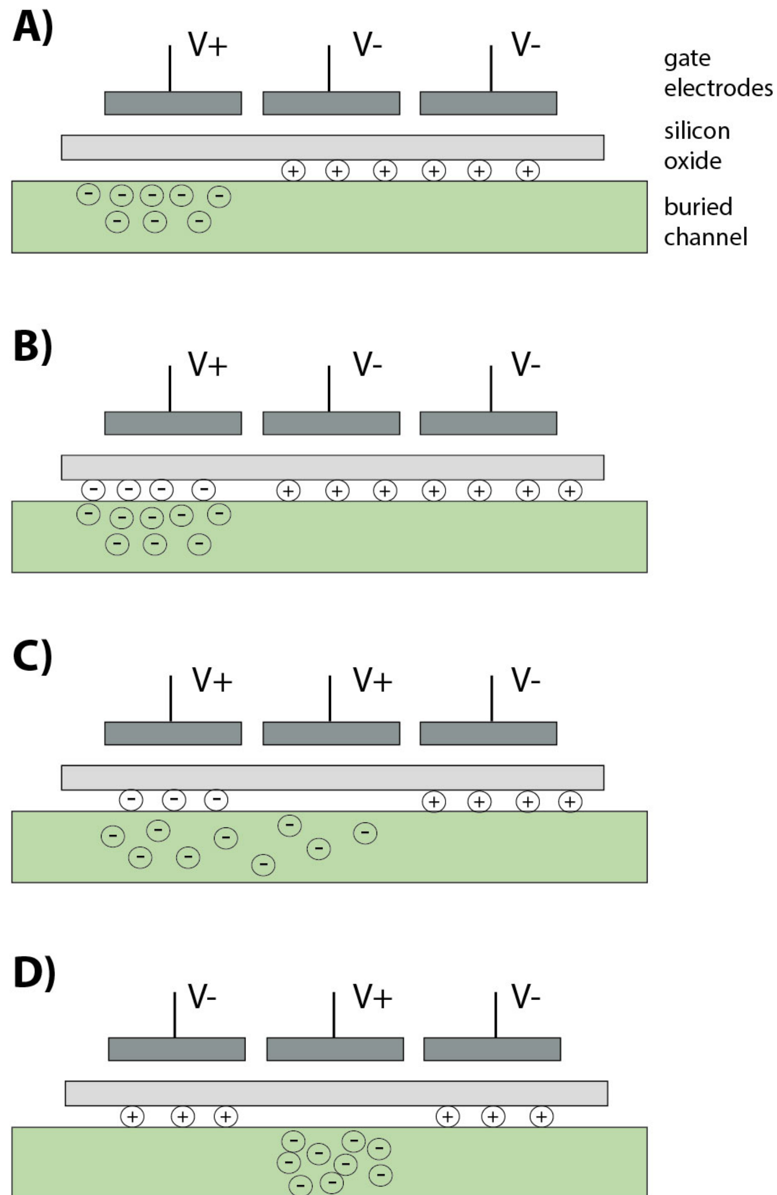

Figure 8.2: Clocked antiblooming mechanism. The signal charges are collected under the gate electrode with the positive potential V+ (A). If the potential well under the collecting gate electrode is saturated, the excess charges accumulate at the silicon-silicon oxide interface (B). Excess charges are trapped at the surface, while the remaining signal charges are shifted in the buried channel to the next gate electrode (C). When the first electrode is clocked into inversion, the trapped charges are annihilated by holes that flood the surface states (D).

8.2 Antiblooming capabilities in pnCCDs

In conventional antiblooming CCDs, the excess charges are siphoned off the device via drain structures integrated into the pixels during fabrication. In contrast to insulated gate CCDs, particularly MOSCCDs, pnCCDs have no closed oxide layer at the register side, which allows removal of electric charges from the device. It was studied by means of numerical device simulations, if it is possible to establish charge drains in the electric potential of the pnCCD by applying the appropriate operation conditions without modifying the pixel layout or fabrication process. The excess charges are expected to be attracted by the positive electric potential of the charge drains and siphoned off the device via the n-channel MOS registers, which are connected to the n-doped inner substrate contacts at the sides of the pixel array. Electrons can be drained off the device, if the electric potential of the pixel structure enables the electrons to reach the surface of the register side and then the inner substrate contacts at the sides of the pixel array [37].
The electric field geometry of the pixels is mainly determined by three operation voltages: the register voltage, the MOS voltage and the back contact voltage. The register voltages determine the size and depth of the potential well and the location where the signal charges are stored. The n-channel MOS registers define the electric potential at the surface regions between the p^+-registers. The back contact voltage has an influence on the storage depth of the signal electrons (section 6.3.2).
The charge drain mechanism including the location where the overflowing signal electrons are removed from the pixel, were studied by cuts through the electric potential in the channel direction through the middle of the channel stop and channel notch implants (figure 8.3).
Figure 8.4 shows the electric potential for cuts in the channel direction through the channel notch and channel stop implants. In figure 8.4A, the operation voltages for the high charge handling capacity mode and in figure 8.4B the operation voltages for the antiblooming mode were applied. Since in the experiments, the signal charges are stored under two registers during integration time, the simulations were also performed for storage under two registers. In the simulations, no signal charges were inserted into the pnCCD.

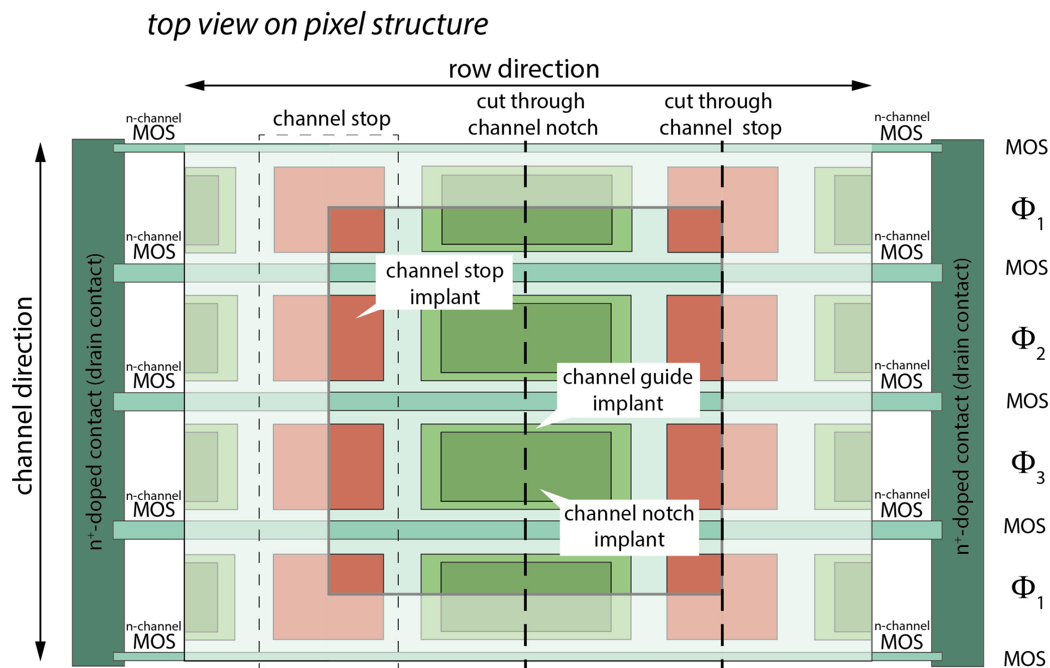

Figure 8.3: Position of the simulated cuts in the channel direction. The simulated cuts through the electric potential of the device follow the channel direction through the middle of the channel stop and channel notch implants.

In the following, the differences between the high charge handling capacity mode introduced in section 6 and the antiblooming mode are presented. In high charge handling capacity mode, the pixel full well capacity is increased by shifting the potential minimum of the signal electrons closer to the register side. This is achieved by applying a more negative difference between the back contact voltage and the register voltage than in standard operation mode. Furthermore, a negative voltage is applied to the MOS contacts, which pushes the electrons away from the surface, so that they stay in their potential wells (figure 8.4A). An additional potential barrier between the pixels is generated and the pixel full well capacity is increased.
In antiblooming mode, an extremely negative voltage is applied to the back contact voltage and 0 V or a positive voltage is applied to the MOS contacts (figure 8.4B). In contrast to the high charge handling capacity mode (figure 8.4C), the electric potential under the MOS contacts between the channel stop implants is now attractive for electrons (figure 8.4D).
In high charge handling capacity mode, the electrons are pushed into their potential minimum by the lateral gradient of the electric potential before they can reach the surface of the register side (figure 6.3).

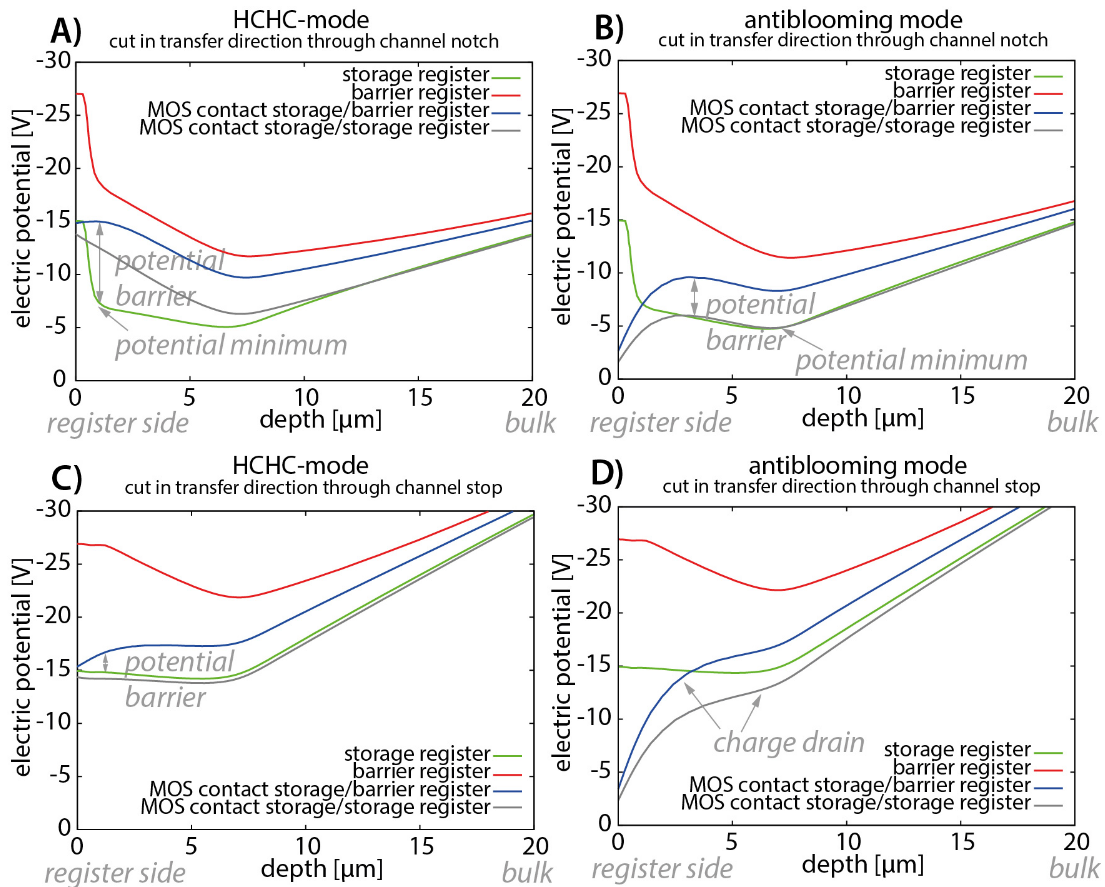

Figure 8.4: One-dimensional cuts through the electric potential in HCHC-mode and antiblooming mode for storage under two registers. In the channel direction the cuts through the middle of the channel guide and channel stop are simulated. A) Cuts through the channel notch and B) channel stop in HCHC-mode. The electric potential prevents electrons to reach the surface of the register side. In the antiblooming mode, the cuts through the channel notch are depicted in B) and through the channel stop in C). If the electrons are stored under two registers, the path to the register side is more pronounced than for storage under one register.

In antiblooming mode, electrons can reach the register side, since the potential barrier to the register side is lowered between the channel stop implants under the MOS contacts (figure 8.4C).

Under the MOS contacts is an n-doped layer with electron accumulation. Furthermore, the MOS contacts are connected to n-doped implants at the sides of the pixel array. Electrons reaching the register side at the charge drains can move along the thin conducting charge layer under the MOS contacts to the n-doped inner substrate contacts at the sides of the pixel matrix. The path for the signal electrons from their potential minimum to the surface of the register side is especially pronounced under the MOS

contacts between the channel stop implants. The positive MOS voltage increases the conductivity of the charge layer under the MOS contacts by increasing the amount of electrons under the MOS contacts. The inner substrate contact, which is set to 0 V, acts as drain contact and attracts the excess charges. The pnCCD can be switched between the high charge handling mode and the antiblooming capability by applying the appropriate operation voltages.

For non-antiblooming operation modes, the channel stops are on a more negative potential than the region of the channel notch and channel guide implants in the pixel center, where the electrons are stored. They repulse the electrons and form a potential barrier in the row direction. Increasing the potential difference between the register side and the back contact side by applying an extremely negative voltage on the back contact pushes the storage depth of the signal electrons closer to the register side. The potential barrier to the surface of the register side is lowered at the regions of the channel stops and MOS contacts by applying 0 V or a positive voltage to the MOS registers.

Under these conditions, the signal electrons can reach the register side. This mechanism is more effective when the signal electrons are stored under two registers during integration time, since in this case, the potential barrier to the register side is lower, especially in the region of the storage registers (figure 8.4D). Since pnCCDs have no closed oxide layer on the register side, a direct access to the semiconductor is provided and the excess charges can be removed from the device via ohmic contacts. The potential barrier between the storage and the barrier register is reduced in antiblooming mode compared to the HCHC-mode. So, the pixel full well capacity in antiblooming mode is significantly reduced compared to the HCHC-mode. In antiblooming mode, approximately 3×10^5 electrons can be stored in one pixel before they spill over the pixel border and are siphoned off. The locations of the charge drains in the pixel structure are marked in figure 8.5. The charge drain is stronger in the pixel center between the two storage registers (Φ_2 and Φ_3) than between a storage and a barrier (Φ_1) register. This is indicated by larger yellow boxes in figure 8.5.

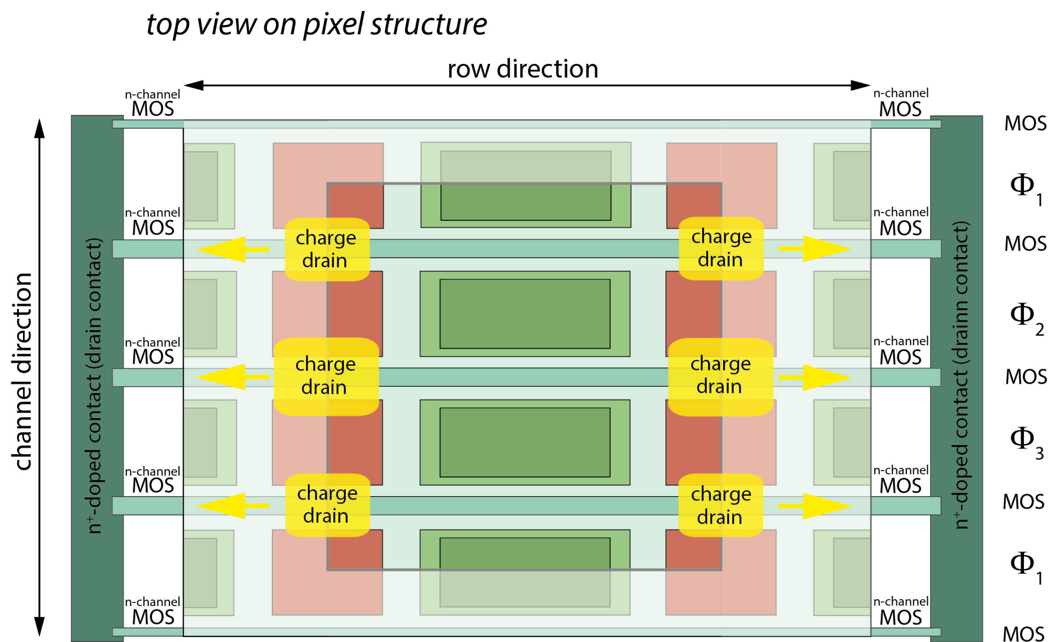

Figure 8.5: Charge drain in antiblooming mode for storage under two registers. In antiblooming mode, the surplus signal charges are drained to the n-doped inner substrate contacts at the sides of the pixel array via the channel stops and the MOS structure, before they spill into neighboring pixels. So, the inner substrate contacts act as drain contacts. With the applied voltages, the electric potential is modified to generate charge drains in the pixel structure, which are highlighted in yellow. N-implants are under the MOS contacts, and the MOS contacts are connected to the n-doped inner substrate contacts at the sides of the pixel array. Excess charges are drained to the n-doped inner substrate contacts on both sides of the device via MOS registers, before they spill into adjacent pixels (yellow arrows). The charge drain is stronger in the pixel middle between the two storage registers (Φ_2 and Φ_3), which is indicated by larger yellow boxes.

The signal charges are drained to the inner substrate contacts at the sides of the pixel array during integration time. The charge drain mechanism is more effective for storage under two registers than for storage under one register during integration time. Since the transfer registers and the MOS registers are in the direct vicinity, the electric potential under the p^+-registers affects the electric potential under the MOS registers and vice versa. If the electrons are stored under two registers in antiblooming mode, the electric potential under the MOS registers is shifted to more positive values than for storage under one register. The reason is that the two neighboring storage registers result in a more positive potential than a storage and a barrier register (figure 8.6). Furthermore, the negative charged signal electrons shift the electric potential under the registers to more negative values (section 6.3.2). Since the potential well, in which the electrons are stored, has a larger area for storage under two registers, the electric potential is

shifted to less negative values than for storage under one register. This supports the charge drain via the n-channel MOS contacts, which are connected to the n-doped inner substrate contacts for storage under two registers. The experimental confirmation of the simulation results is presented in section 12.1.

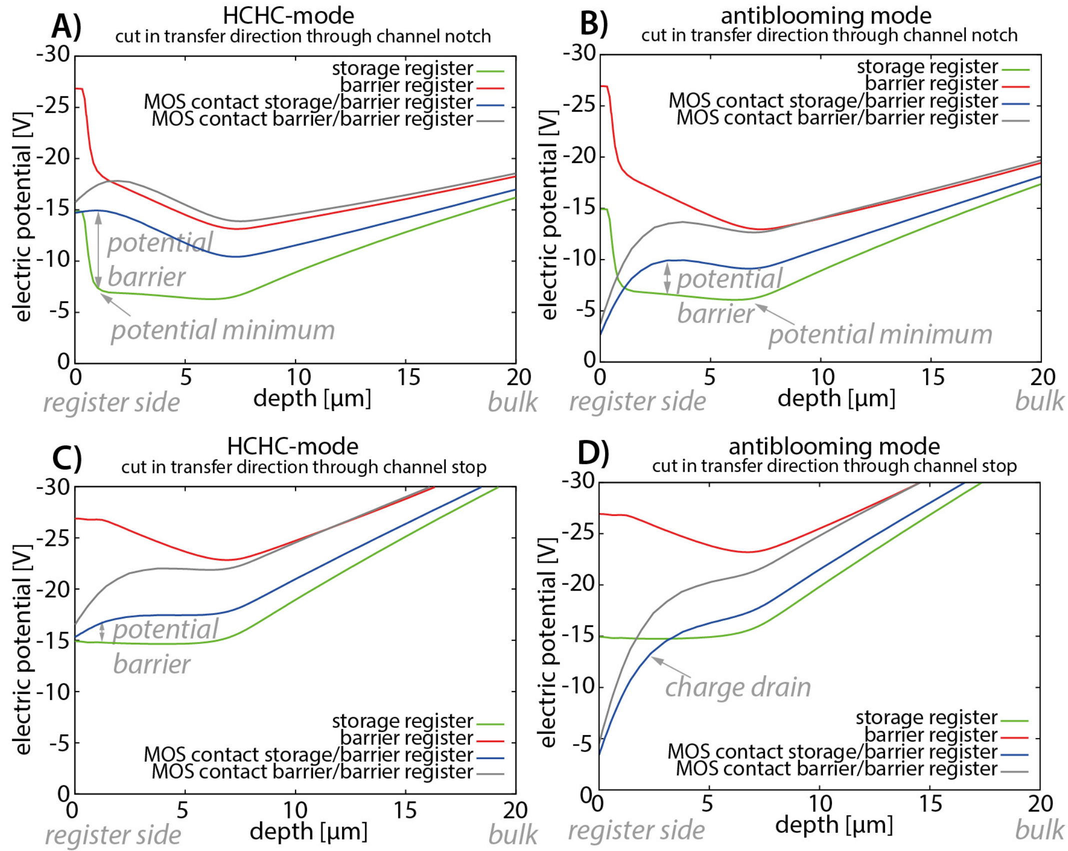

Figure 8.6: One-dimensional cuts through the electric potential in HCHC-mode and antiblooming mode for storage under one register. In the channel direction, the cuts through the middle of channel guide and channel stop are simulated. A) Cuts through the channel notch and C) channel stop in HCHC-mode. The electric potential prevents electrons from reaching the surface of the register side. In the antiblooming mode, the cuts through the channel notch are depicted in B) and through the channel stop in D). The electric potential allows electrons to reach the surface of the register side via the channel stops.

Summary of chapter 8

An activatable charge extraction mechanism for pnCCDs was presented. An extremely negative back contact voltage in combination with a positive MOS voltage reduces the potential barrier to the surface of the register side under the MOS registers between the channel stop implants. The channel stops form the potential barrier between the pixels in the row direction, the dominant charge spilling direction. Instead of spilling into adjacent pixels, the charge is siphoned off to the register side and pulled to the inner substrate contacts at the sides of the pixel array via the thin conducting charge layer under the MOS contacts.

9 Experimental methods

9.1 The pnCCD setup

The simulation results were experimentally confirmed with a laser setup, which was purpose-built for the study of the dynamic range of pnCCDs. The light of the optical laser was used to simulate X-rays. With the laser, signal charges were injected into the pixels of the pnCCD and the charge spilling was quantified.
The setup consists of a vacuum chamber with two independent parts. The first part is used for operating the pnCCD detector and the second part contains different kinds of radiation sources. The pnCCD vacuum chamber contains the focal plane with the pnCCD and permits a stable operating environment for the detector. In order to keep the leakage current negligible small even at slow readout speeds, the pnCCD is cooled to temperatures of down to -50 °C. The detector is cooled with a stirling cooler, which is coupled to the pnCCD via a cooling mask made of copper. In order to prevent the formation of ice on the detector, the pnCCD is operated at pressures of approximately 10^{-5} Pa. Icing on the detector can lead to short circuits and to the destruction of the device. A low pressure inside the chamber also prevents the absorption of X-rays in air. The pnCCD and the readout ASIC CAMEX are mounted on a ceramic board (figure 9.1). The ceramic board is connected to the so-called inner electronic board via a Zero Insertion Force (ZIF) socket. Since the pulse drivers for the register voltages and RC (Resistor-Capacitor) filters for the minimization of electronic disturbances as well as the output amplifier have to be located near the pnCCD, they are elements of the inner electronic board. The outer electronic board is located outside the vacuum chamber. It includes the analog and digital signal drivers and the cable connectors. The operation voltages for the pnCCD and CAMEX are supplied by ultra-low noise power supplies. In order to keep the common mode fluctuations, which is the linewise variation of the electric baseline, to a minimum, the supply voltages have to be extremely stable. The digital timing signals, which are needed to operate the pnCCD and CAMEX chip, are delivered by a time pattern generator, the so-called sequencer.

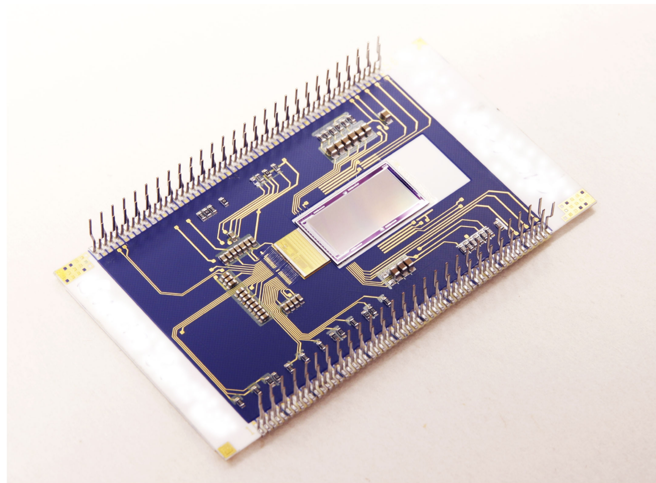

Figure 9.1: pnCCD on ceramic board. The pnCCD and the readout ASIC CAMEX are mounted on a ceramic board and connected via wire bonds. The 110 pins of the ceramic board are plugged into the zero insertion force socket of the inner board.

The sequencer also synchronizes the ADC (Analog Digital Converter) and the data acquisition system.
The chamber part with the radiation sources contains the laser setup and a radioactive ^{55}Fe source, which is used for detector calibration and evaluation of the spectroscopic performance of the pnCCD.
The wavelength of the laser is 635 nm. The laser light is coupled into the chamber with an optical fiber. The fiber is connected to a micro-focus optics, which is mounted on compact micro-translation stages with a stepping size of 2 µm. The pnCCD is illuminated with a focused laser spot with a Gaussian profile and a spot diameter of 5 µm full width at half maximum (FWHM) (figure 9.2). Since the laser spot is small compared to the pixel size, it is possible to move the laser spot over pixel borders and to illuminate each pixel of the pnCCD separately, by moving the optics via motor stages. The optical photons hit the detector at the entrance window and create electron-hole pairs in the silicon bulk. The number of generated charges can be varied by means of an optical attenuator and the width of the laser pulse.

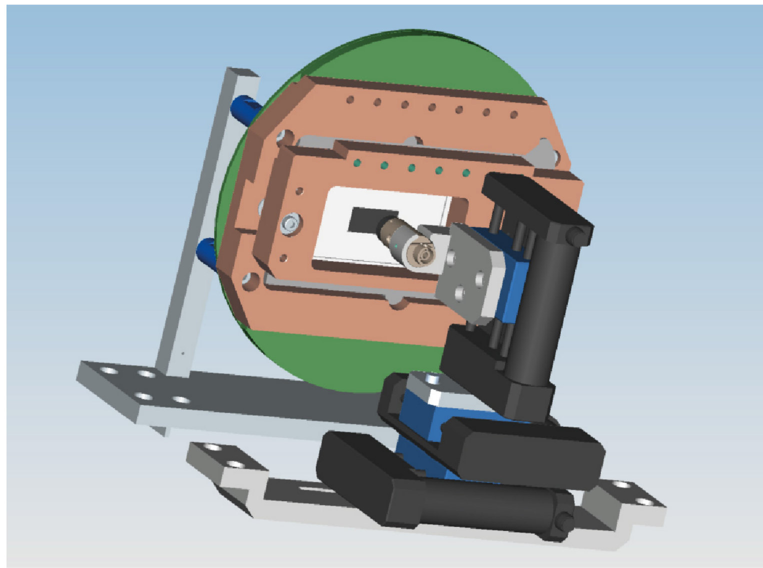

Figure 9.2: Schematic of the laser setup. A laser with a wavelength of 635 nm is focused on the pnCCD entrance window by means of a micro-focus optics and micro-translation stages. By increasing the laser intensity stepwise, the charge spilling into neighboring pixels is studied.

The number of both optical and X-ray photons decreases exponentially as function of the penetration depth in the detector material. For optical photons with a wavelength of 635 nm, the attentuation length in silicon is approximately 1.5 µm. The absorption of photons is a statistical process involving secondary processes like fluorescence excitation and Compton scattering. The statistical fluctuation of the deposited energy per unit path length is negligible if a few hundred photons are absorbed at the same time. Therefore, the laser simulates the energy distribution of many X-rays, not the absorption of individual X-ray photons. The anti-reflective coating deposited on the photon entrance window results in a high quantum efficiency of approximately 95%-100% for optical photons (figure 9.3). At a wavelength of 635 nm, one photon generates one signal electron in the bulk [12]. Therefore, approximately 280 optical photons generate the same amount of signal charges as one X-ray photon with an energy of 1 keV.
For detector calibration, a radioactive ^{55}Fe source is used as described in the following section.

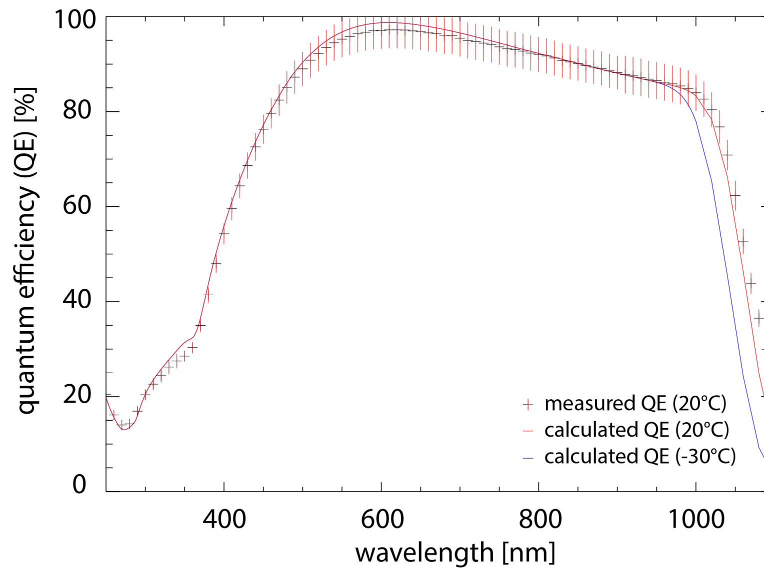

Figure 9.3: Quantum efficiency of pnCCDs in the optical region. Measured and calculated quantum efficiency of an entrance window with the anti-reflective coating used by pnCCDs. The quantum efficiency was determined for optical and infrared photons for room temperature and a temperature of -30 °C.

9.2 Data analysis

In order to be able to analyse the data of the laser measurements, the pnCCD has to be calibrated for each set of operation parameters to determine the amplification factors of each readout channel. In this section, the filtering, correction and analysis of the raw data are explained.

9.2.1 Detector calibration

The pnCCD data acquisition system writes the raw data in a binary format. The files contain a file header and per frame a frame header, followed by the complete data of the frame, consisting of the position and amplitude of the photon event. For each frame, the signal of each pixel in ADU (Arbitrary Digital Units) is stored. The data can be either evaluated online with a C-based analysis tool called X-online or offline, with an offline analysis program written in the programming language IDL (Interactive Data Language) [38].

In each measurement, signal frames and dark frames are written. The dark frames

consist usually of 200 frames, which are not illuminated with photons. From these dark frames, offset and noise are calculated. The offset represents the quiescence level of each pixel. It is calculated individually for each pixel as the average over all calibration frames. The offset results from two effects. First, during charge collection, each pixel accumulates leakage current, caused by thermally generated electron-hole pairs shifting the signal baseline. Second, each readout channel shows an offset. The offset correction is applied by substracting the averaged pixel-wise ADU signal of all dark frames from the signal frames. As a next step, a common mode correction is performed for the signal frames. The common mode is a time dependent bias, which is common to all pixels in a row. It is caused by external electromagnetic disturbances during the readout of a line. As long as the number of photons per row is much smaller than the number of pixels in the respective row, it is corrected by substracting the median of each row in each frame. The median is a location parameter. It is the value separating the higher half of a data sample, from the lower half. The advantage of the median in describing data compared to the mean value is that it is a robust estimator, thereby not as sensitive to outliers in the data. Even without the presence of a radiation source, there is always a low background rate of so-called Minimum Ionizing Particles (MIPs), mainly cosmic muons. To minimize the influence of the background induced by MIPs on the calculated noise value, the five highest noise values for each pixel within the calibration frames are discarded. In order to prevent the noise from being systematically shifted to lower values, the five lowest values are also discarded. By using the common mode corrected dark frames, the standard deviation is determined pixel wise, forming the noise map. The noise threshold level affects the minimum photon energy that can be distinguished from the dark noise and causes a broadening of the energy peak.
The data of the laser measurements are offset corrected. After the correction is performed, the individual signal of the illuminated pixels is determined, as well as the integrated signal over the illuminated spot. In order to calibrate the detector, the amplification factors of the individual readout channels of the pnCCD system are determined. The signals of the pnCCD are processed in parallel in all 128 channels of the CAMEX. Each channel has its own amplification chain consisting of a first FET, the CAMEX amplifier and a sample and hold stage. Thus, it has its own amplification properties, the so-called gain and the differences in the signal amplification of the different channels must also be corrected. For calibration measurements, the detector is illuminated in flatfield with a radioactive ^{55}Fe source. The radioactive source is used to provide a homogeneous illumination with photons of defined energy. ^{55}Fe decays by electron capture to ^{55}Mn and emits radiation with an energy of $E_{K_\alpha} = 5.89\,\mathrm{eV}$ and, with significantly lower intensity, $E_{K_\beta} = 6.49\,\mathrm{eV}$. The Mn K_α line of the ^{55}Fe source

generates a certain number of electron-hole pairs (approximately 1620), which is used to convert the laser signal in ADU into the number of generated signal electrons. The conversion factors for the amplification and the number of samples of the multi-correlated double sampling, have to be taken into account. Because of the high signal amplitude, the lowest gain and only two samples of the eight possible samples of the correlated double sampling are taken. However, the calibration measurements are performed with the second highest gain and eight samples.

In order determine the amplitude of the Mn K_α line, further data processing steps are required. To distinguish the photon signals from the noise fluctuations, all pixel values above a defined threshold are selected from the offset and common mode corrected signal frames. The detection threshold is chosen to be four times the mean readout noise (root mean square) of the pixel. The selected pixels are recombined by summing up the charge content of neighboring pixels in photon events whose signal charges have spread over multiple pixels. According to the distribution of the signal amplitude and their position to each other, they are classified as valid or invalid events. The valid events are categorized as singles, doubles, triples and quadruples. By the invalid pattern, MIPs, pileup events and noise excesses are removed.

After event analysis, charge transfer losses and the different amplifications of the readout channels are corrected. During the charge transfer along the channel, electrons can be trapped by impurities in the silicon wafer, causing so-called charge transfer losses. The CTE model assumes that for each transfer a fraction of signal charges in the pixel is lost. With increasing distance to the readout, the amount of charge losses increases and the peak position, which is related to the amount of signal charges, is shifted to lower energy values. The charge transfer efficiency is determined from fitting the spectrum peak position row-wise. For the CTE correction, only single events are used.

Finally, all valid events are combined to a spectrum and the obtained amplitude is used to calibrate the laser measurements.

9.2.2 Measurements using a laser diode

The evaluation of the laser measurements is based on the IDL offline analysis. 200 dark frames and 200 signal frames were recorded for each laser measurement. Offset and noise correction are performed on the signal frames. A common mode correction is not applied, as there is a very high signal in only a few pixels, which would distort all data in the row. For each frame, the signal in the center pixel, which is illuminated by the laser, the signals of its neighbors and the integrated signal over the whole laser spot are determined and averaged over the number of signal frames.

Laser diodes tend to do mode hopping, which results in power noise and a stochastic variation of the wavelength. The laser diode used was originally developed for applications in optical metrology. It has a noise of less than 0.1% RMS (Root Mean Square) and a small speckle contrast. The speckle contrast is defined to be the ratio between the standard deviation of the intensity and the mean of the intensity. This light source guarantes a stable and homogeneous signal over the entire laser spot. Thus, the intensity variation between the different pixels is extremely small. The conversion of the signal in ADU to the number of generated electrons is performed with the aid of calibration measurements. The gain factor and the number of signal samples are taken into account.

9.3 Tested pnCCDs

The pnCCDs used in this study, were developed within a collaboration of PNSensor GmbH and the semiconductor laboratory of the Max Planck Institute for extraterrestrial physics. They have a pixel size of 75 µm × 75 µm and an image area of 128 × 256 pixels. The pnCCDs can be operated in frame store mode as well as in full frame mode. For the measurements presented here, the pnCCDs were read out in full frame mode with a readout speed of 20 Hz. In spectroscopic measurements, noise levels of down to 2.5 electrons (RMS) and a full width at half maximums of down to 135 eV were achieved using the pnCCD auto-reset. These measurements were performed in the second highest gain mode. The charge transfer inefficiency is as low as 10^{-5}. The detectors were read out with a 128 channel CAMEX. All pnCCDs with a pixel size of 75 µm × 75 µm used in this study have the same pixel geometry. But they differ in the resistivity of the silicon substrate and thus have different depletion voltages. This affects the storage depth of the signal electrons for the same operation voltages and, according to the capacitor model of the pixel full well capacity, the charge collection capacity (section 6.3.1). Furthermore, the influence of the space charge distribution in the pnCCD was studied by using different implantation doses for the channel notch, channel guide and channel stop. A higher pixel full well capacity causes higher signal amplitudes, resulting in a higher voltage swing at the readout anode. So, the dynamic range of the pnCCD can also be limited by the on-chip electronics. In order to increase the maximum swing of the readout anode, an additional electric capacitance was integrated in one of the pnCCDs and the influence of the total anode capacitance on the measured signal amplitude was studied.

The influence of the area under which the electrons are stored on the charge handling

capacity was studied with pnCCDs with a pixel size of 48 µm × 48 µm. The pnCCDs with a pixel size of 48 µm × 48 µm have an image area of 264 × 264 pixels and are read out in frame store mode with four 132 channel CAMEX ASICs. The pixel layout of the pnCCDs with a pixel size of 48 µm × 48 µm is optimized for spectroscopic measurements. Therefore, the area of the channel notch, under which the electrons are preferably stored, does not scale with the pixel size. Compared to pnCCDs with a pixel size of 75 µm × 75 µm, it is significantly smaller to minimize charge losses due to defects in the silicon (section 6.3.3).

The following pnCCDs were used in this study:

- **CCD 1**: The first pnCCD has a low resistivity silicon substrate and consequently a high depletion voltage. The ion implantation dose of the n-channel guide and n-channel notch are lower than in CCD 2, whereas the p-type implantation of the channel stop has a higher dose. CCD 1 corresponds to the standard pnCCD used for spectroscopy. The standard ion implantation dose of the n-implants was chosen.
- **CCD 2**: The second pnCCD is built on high resitivity silicon and thus has a lower depletion voltage. The ion implantation dose of the n-channel guide and n-channel notch is higher than the standard ion implantation dose used in CCD 1. The ion implantation dose of the p-channel stop is lower.
- **CCD 3**: The third pnCCD is equal to CCD 1, except for the higher electric capacitance of the readout anode.
- **CCD 4**: The fourth pnCCD has a pixel size of 48 µm × 48 µm. The process parameters and the bulk material are identical to CCD 1.

Summary of chapter 9

In this chapter the pnCCD test setup containing a laser setup and a radioactive ^{55}Fe was described. Furthermore, a short introduction to the analysis and calibration of the data was given. Finally, the tested pnCCDs and their differences in layout and production parameters were presented.

10 Experimental and theoretical analysis of the pixel full well capacity

10.1 Effect of the operation voltages

The device simulations showed that the charge handling capacity can be increased by increasing the electric potential barrier between the pixels and decreasing the storage depth of the signal electrons. The potential barrier between adjacent pixels is determined by the register voltages and the MOS voltage. The back contact voltage has an influence on the storage depth. A more negative back contact voltage shifts the potential minimum of the signal electrons closer to the register side. Inreasing the Φ-amplitude of the transfer registers increases the potential barrier between adjacent pixels. A more negative MOS voltage pushes the electrons away from the register side and prevents electrons to be absorbed to the inner substrate in the regions between the p^+-registers. Additionally, a negative MOS voltage increases the potential barrier between neighboring pixels (section 6.1).

In order to study the influence of the back contact voltage on the electric potential experimentally, the absolute value of the back contact voltage was increased from -230 V, used in standard operation mode, to -400 V (figure 10.1). The register and back contact voltages are held at the values for the HCHC-mode determined by the device simulations (Φ-offset: -14 V, Φ-amplitude: -12 V, MOS: -15 V). For each voltage set, 7×10^5 electrons were generated inside the pnCCD (here CCD 1) with an optical laser. All signal electrons were generated in the center pixel in which the laser spot was focused. The signal of the pixel, in which the laser spot was focused, was quantified, as well as the integrated signal over all pixels filled with signal electrons.

Figure 10.1A shows cuts through the electric potential through the middle of the storage register in the channel direction. The electric potential of CCD 1 was simulated for different back contact voltages. For CCD 1, a lower ion implantation dose of channel guide and channel notch and a silicon bulk with a lower resistivity than CCD 2 were used (section 9.3). No signal charges were injected in the simulations. In figure 10.1B,

the corresponding one-dimensional cuts through the barrier register for simulation in the channel direction are shown.

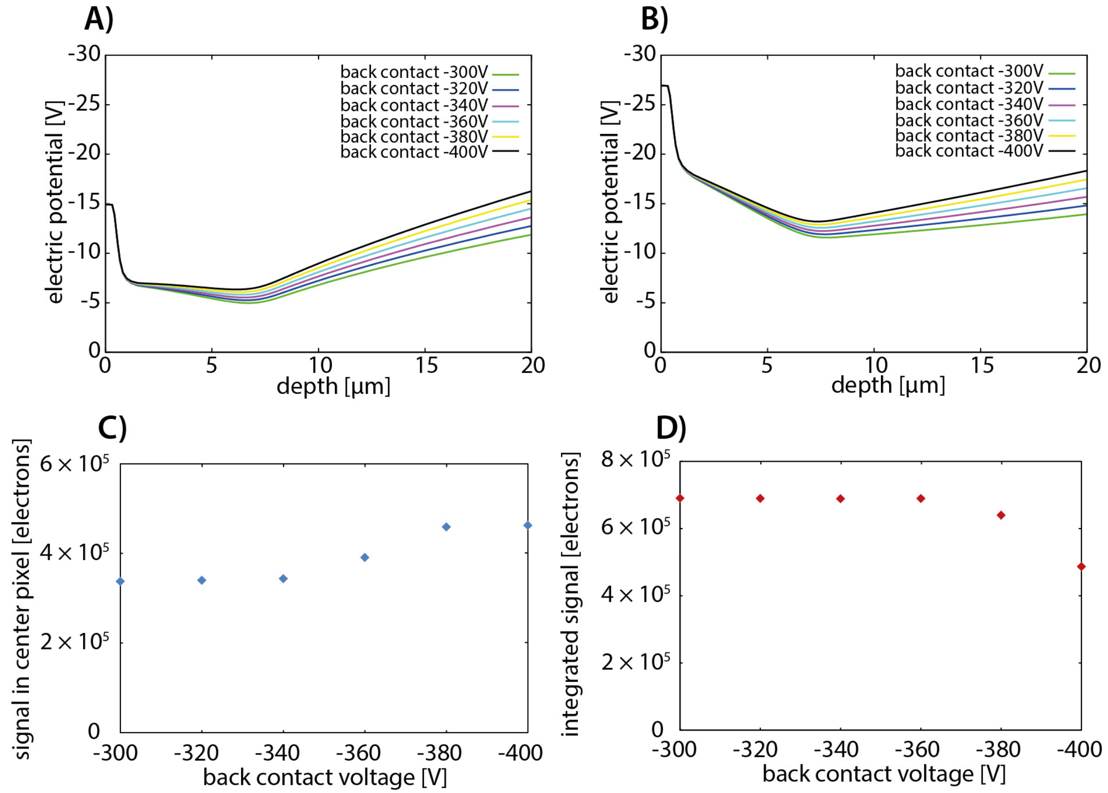

Figure 10.1: Simulation and experimental results for variation of the back contact voltage. The electric potential is simulated for a cut in the channel direction. A) One-dimensional cuts through the middle of the storage register. B) Cuts through the middle of the barrier register. C) Measured signal of the pixel, in which the laser spot is focused. D) Integrated signal over all pixels filled with signal charges.

As already discussed in section 6.1, a more negative back contact voltage shifts the global potential minimum for electrons, which is at a depth of 7 µm, to more negative values until it is on approximately the same level as the electric potential at a depth of 1.4 µm. A magnified view of the electric potential at a depth of 7 µm is shown in figure 10.2. The increase of the pixel full well capacity starts for back contact voltages between -300 V and -400 V. By applying a back contact voltage of -400 V, the electric potential of the storage register (figure 10.2A) at a depth of 7 µm is 5.4 V more negative than for a back contact voltage of -300 V. Figure 10.2B shows the electric potential of the barrier register for variation of the back contact voltage. The electric potential here is shifted by the same value.

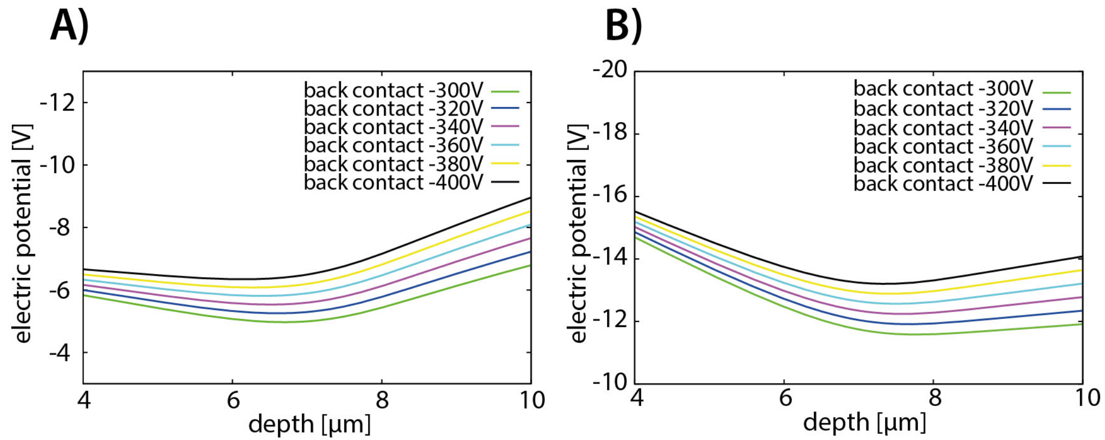

Figure 10.2: Electric potential for variation of the back contact voltage. The electric potential is simulated for a cut in the channel direction. The region of the potential minimum at a depth of 7 µm of figure 10.1 is scaled up. A) One-dimensional cuts through the middle of the storage register. B) Cuts through the middle of the barrier register.

The potential barrier between the global potential minimum at a depth of 7 µm and the electric potential at a depth of 1.4 µm is reduced and the signal electrons are stored closer to the register side, increasing the charge handling capacity of the pixels.

The dependence of the charge handling capacity of CCD 1 on the back contact voltage can be determined from figure 10.1C and figure 10.1D. In figure 10.1C the signal of the center pixel, in which the laser spot is focused, is plotted as a function of the applied back contact voltage. The MOS contact is set to -15 V, Φ-offset is -14 V and Φ-amplitude is -12 V. The number of generated signal charges is 7×10^5. No common mode or gain corrections were applied on the data. Up to a back contact voltage of -340 V, the signal in the center pixel corresponds to approximately 3.2×10^5 electrons. The signal charges are spread over five pixels, three of which are completely filled with electrons. For a back contact voltage more negative than -340 V the signal in the center pixel rises until it reaches a value of approximately 5×10^5 electrons for a back contact voltage of -380 V. It stays constant until a back contact voltage of -400 V is reached. Thus, for a back contact voltage of -340 V, the storage depth starts to be shifted closer to the register side. The potential difference between the global potential minimum at a depth of 7 µm and the electric potential at a depth of 1.4 µm is now small enough that signal electrons can move from the bulk towards the surface of the register side. A more negative back contact voltage further decreases the potential barrier to the register side and more electrons are stored closer to the front side, which increases the charge handling capacity.

The negative charges of the signal electrons in the center pixel further decrease the potential barrier between the electric potential at a depth of 1.4 µm and the global potential minimum at a depth of 7 µm, in which the electrons are preferably stored (section 6.3.2). In figure 10.1D, the integrated signal over all pixels filled with signal electrons is plotted against the back contact voltage. By applying a more negative back contact voltage, the pixel full well capacity increases and the number of pixels, in which the electrons are stored, decreases until all electrons are stored in only one pixel. As soon as the signal in the center pixel corresponds to approximately 5×10^5 electrons, the integrated signal decreases from 7×10^5 electrons to 5×10^5 electrons for a back contact voltage of -400 V. This is due to the fact that the on-chip electronics cuts the electron signal in the remaining pixel filled with electrons at the value mentioned above. The reason is that the maximum voltage swing that the gate of first FET of the center pixel can process corresponds to 5×10^5 electrons for this CCD channel. A more detailed explanation is given in section 13.1. Thus, the maximum value of the electron signal that can be read out is not limited by the charge handling capacity, but by the dynamic range of the readout electronics.

In figure 10.3, the dependence of the charge handling capacity on the MOS voltage was studied. Therefore, a back contact voltage of -400 V, a Φ-offset voltage of -14 V and a Φ-amplitude voltage of -12 V were applied. Figure 10.3A shows cuts through the electric potential through the middle of the storage register in the channel direction for the variation of the MOS contact voltage. Figure 10.3B shows the corresponding one-dimensional cuts through the barrier register.

A more negative MOS voltage increases the electric potential barrier between the pixels. Furthermore, it shifts the global potential minimum at a depth of 7 µm to more negative values. The potential barrier between the global potential minimum and the electric potential at a depth of 1.4 µm is lowered and electrons can be stored closer to the register side increasing the pixel full well capacity.

A magnified view of the electric potential at a depth of 7 µm is shown in figure 10.4. By applying a MOS voltage of -15 V, the electric potential of the storage register (figure 10.4A) at a depth of 7 µm is 2.4 V more negative than for a MOS voltage of -3 V. Figure 10.4B shows the corresponding electric potential of the barrier register. In figure 10.3C and figure 10.3D, 7×10^5 electrons were generated inside the pnCCD with a laser focused on the center pixel of the spot. The MOS voltage was decreased in 3 V steps from -3 V to -15 V and the signal of the pixel in which the laser spot was focused and the integrated signal over all pixels filled with signal charges are plotted.

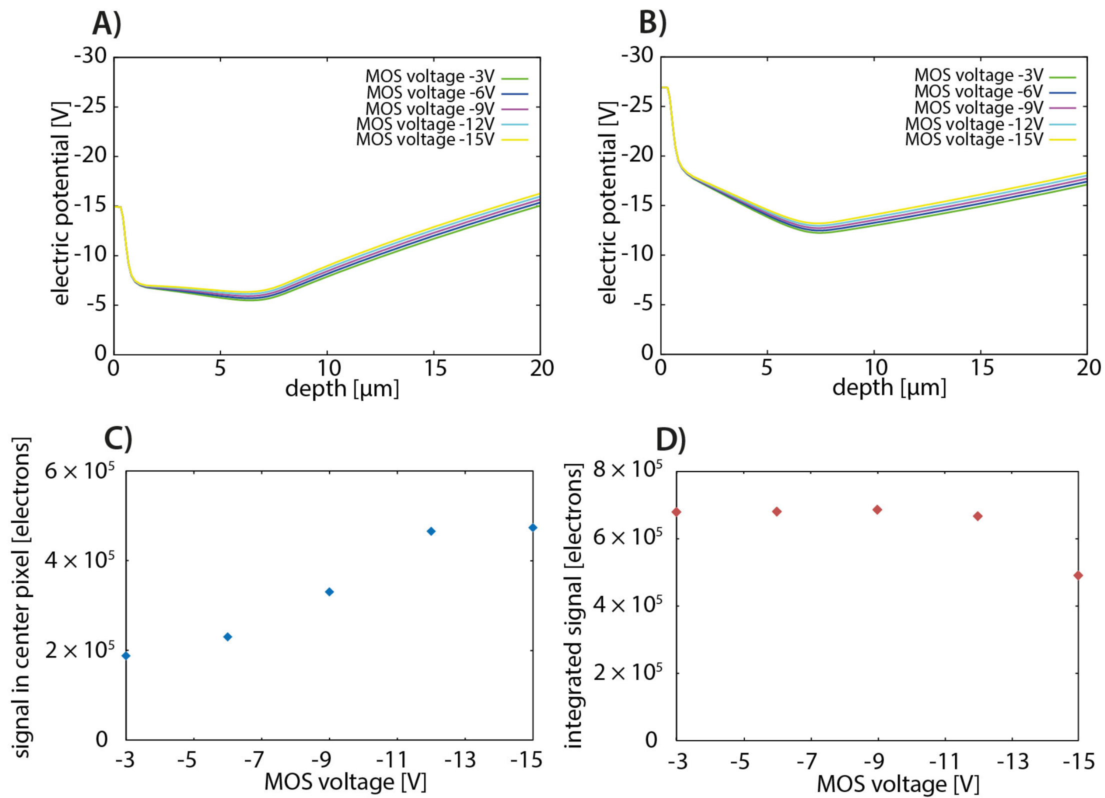

Figure 10.3: Simulation and experimental results for variation of the MOS voltage. In A) and B) simulations of the electric potential in the channel direction were performed. A) One-dimensional cuts through the middle of the storage register. B) One-dimensinal cuts through the middle of the barrier register. C) Signal of the pixel, in which the laser spot is focused. The amount of signal charges generated by the chosen laser intensity is below the limit of the readout electronics. D) Integrated signal over all pixels filled with signal charges.

The signal in the center pixel increases with decreasing MOS voltage up to approximately 5×10^5 electrons and the number of pixels, in which the signal charges spill over, decreases since the potential barrier between the pixels is increased and the storage depth is shifted closer to the register side. If -13 V or a more negative MOS voltage is applied, the signal integrated over the laser spot decreases. Due to the limitation of the readout electronics, the signal amplitude of the pixels is cut at a certain value, which corresponds to the maximum voltage swing of the first FET. For CCD 1, the signal amplitude is cut at 5×10^5 signal electrons. The fact that the maximum measured signal amplitude of the pixels does not correspond to the maximum charge handling capacity of the pixels is due to the limitation of the on-chip electronics. The dynamic range of a pixelated detector is consequently a combination of the pixel full well capacity and the dynamic range of the readout node.

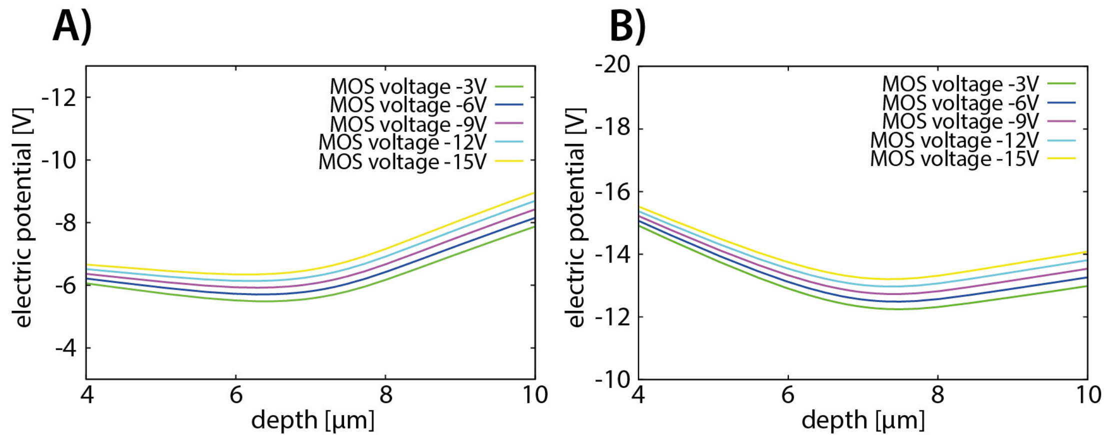

Figure 10.4: Electric potential for variation of the MOS voltage. In A) and B) simulations of the electric potential in the channel direction were performed. The region of the potential minimum at a depth of 7 µm of figure 10.3 is scaled up. A) One-dimensional cuts through the middle of the storage register. B) One-dimensinal cuts through the middle of the barrier register.

In figure 10.5, 1.8×10^6 signal electrons are generated. In standard operation mode, there is a charge spilling over several pixels, since the charge handling capacity is 3×10^5 electrons (figure 10.5A). In HCHC-mode (figure 10.5B), all signal charges are stored in one pixel, but the measured signal corresponds to 5×10^5 electrons only, which is the limit of the on-chip electronics of the center pixel.

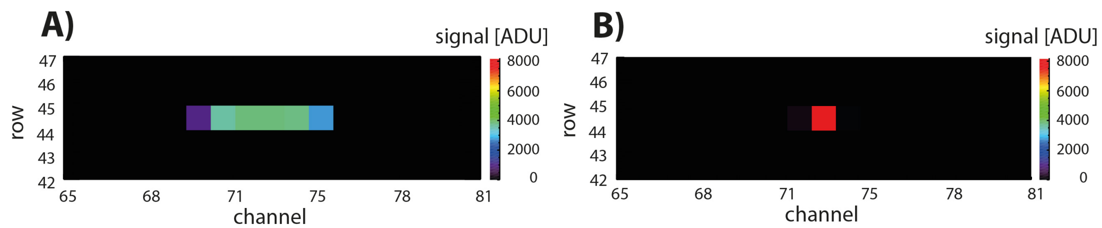

Figure 10.5: Charge distribution of CCD 1 in different operation modes. In both cases the amount of generated signal electrons is 1.8×10^6, but the operation voltages are different. In standard operation mode (A), the charges spill over several pixels since the amount of generated signal charges exceeds the pixel full well capacity. In HCHC-mode (B), there is no charge spilling. Due to the limitation of the maximum swing of the readout electronics the signal is cut at an amplitude of about 8×10^3 ADU, which is equivalent to approximately 5×10^5 signal electrons.

This effect is also illustrated in figure 10.6 by using CCD 2 (section 9.3). In figure 10.6, the intensity of the laser spot is increased in equidistant steps and the integrated signal over all pixels filled with signal charges is measured, as well as the signal in the center pixel, its neighbors and second neighbors in the row direction, as well as its neighbors

in the channel direction. The signal of the center pixel and the integrated signal increase linearly with increasing number of generated photons. As soon as a value of approximately 7×10^5 electrons is reached, the signal in the center pixel stays constant. Although more than 7×10^5 electrons, which is the limit of the on-chip electronics of the center pixel of the laser spot on CCD 2, are injected in the center pixel, the signal amplitude of the center pixel does not increase and there is no charge spilling into neighboring pixels until 2.8×10^6 signal electrons are generated in the center pixel.

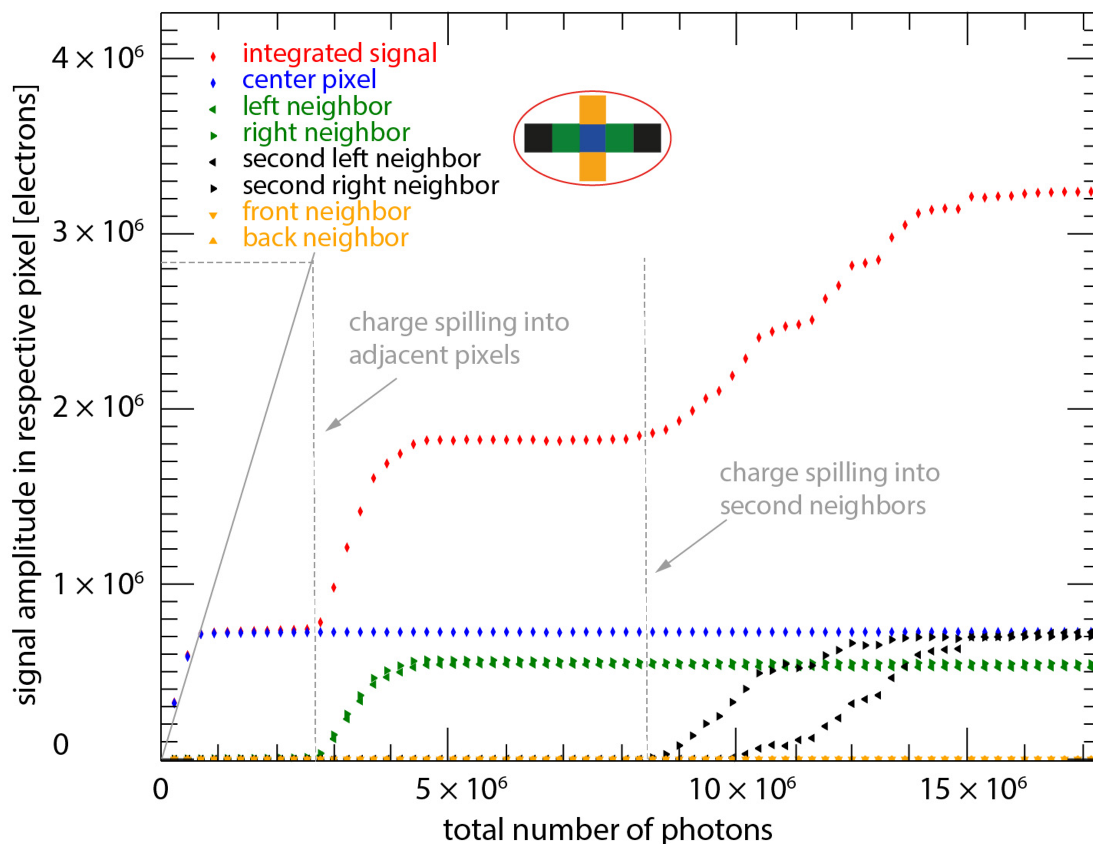

Figure 10.6: Variation of the laser intensity in HCHC-mode. The integrated signal over all pixels filled with signal charges is measured as well as the signal in the center pixel, its neighbors and second neighbors in the row direction, as well as its neighbors in the channel direction. There is no charge spilling in the channel direction. The signal in the center pixel increases with increasing laser intensity. If the maximum charge handling capacity is reached, surplus charges spill over into neighboring pixels. The charge spilling starts at a laser intentity that corresponds to approximately 2.8×10^6 signal electrons. The fact, that the maximum signal does not exceed 7×10^5 electrons is owed to limitations of the readout electronics. The maximum signal height between the center pixel and its neighboring pixels differs, because there was no gain correction applied to the data.

For 2.8×10^6 electrons, the signal charges spill into the neighboring pixels in the row direction. The integrated signal increases since the signal of the neighboring pixels in the row direction increases due to charge spilling. For 8.4×10^6 photons, the signal charges start to spill over into the second neighbors in the row direction. Therefore, the signal electrons exceeding 7×10^5 electrons are stored in the center pixel, but the signal amplitude of the pixel is cut due to limitations of the readout electronics. From the transistor measurements of the first FET it is determined that 7×10^5 electrons correspond to a voltage swing of 2.7 V (section 13.1).
In CCD 2, the maximum signal of the center pixel and its neighboring pixels differs slightly (figure 10.6), because the electric amplification varies between even and odd channels in this pnCCD. Since the readout electronics of the center pixel and its second neighbors have the same signal amplification factor, their signals are both cut at approximately 7×10^5 electrons.
The pixel full well capacity is determined by extrapolation of the signal in the center pixel (figure 10.6). It is 2.8×10^6 electrons for CCD 2. This is in agreement with the simulation result for the charge handling capacity of CCD 2 (section 6.3.1). The same characteristics presented for CCD 2 are observed for CCD 1. Here, the charge handling capacity is 1.8×10^6 electrons (figure 10.5), confirming the simulation results in section 6.2.
The operation voltages have to be optimized carefully, to avoid damages of the device or other components of the system. An extremely negative MOS voltage leads to generation of holes under the MOS registers. Since the transfer registers consist of p^+-implants, a MOS contact voltage that is too negative can create a p-channel transistor and a current between the transfer registers starts to flow. Therefore, the pulse drivers of the system may not be able to supply the currents to load the electrical capacitance of the transfer registers.

10.2 Charge transfer losses

The amount of electrons stored in the potential wells decreases with each pixel transfer, because charges either get lost by being trapped by crystal defects in the transfer depth of the silicon bulk or due to imperfections of the potential structure. Locally existing impurities can capture electrons and release them after a certain time intervall.
The charge transfer efficiency is the mean value of the relative amount of signal charges which are transferred from one pixel to the next (section 3.1). The charge transfer inefficiency is the complementary description (equation (3.2)). In standard operation

mode used for spectrocopy, the CTI is as low as 10^{-5} and the charge transfer losses are negligible. In HCHC-mode, the signal charges are stored and transferred closer to the register side than in standard operation mode. A smaller storage depth increases the probability for defects in the transfer depth. Furthermore, the leakage current is increased, because the electric potential is more pronounced in HCHC-mode, which also increases the detector noise [39].

In order to study, if the charge transfer losses increase in HCHC-mode, the same amount of signal charges was generated in pixels, which are located at different distances from the readout region. A significant increase of the CTI would result in a decrease of the signal amplitude with increasing distance of the pixels to the readout anode, since the number of transfer cycles to the readout anode increases. The charge transfer losses were studied by injecting approximately 3.2×10^5 electrons in pixels with different row numbers for three different channels (figure 10.7). The amount of generated signal electrons is below the maximum number of electrons that can be processed by the readout electronics. There is no systematic variation of the signal amplitude with increasing row number and therefore distance from the readout. Since the data plotted in figure 10.7 are not gain corrected, there is a variation between the signal amplitude in the different channels. The signal amplitude measured within one channel stays constant. Therefore, the CTI does not increase if high amounts of signal charges are processed in HCHC-mode. Because of the high amount of signal charges, the existing traps are saturated without creating a significant charge loss.

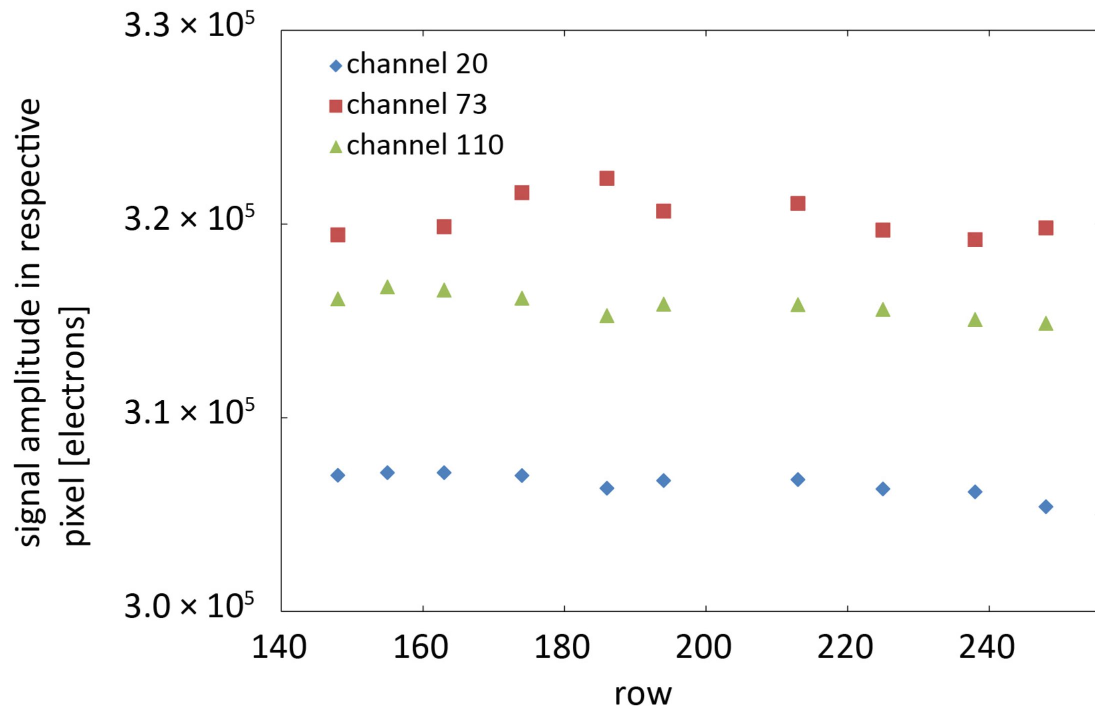

Figure 10.7: Dependency of the signal amplitude on the pnCCD row. The laser spot was focused in pixels with different distances from the readout. There is no decrease in the signal amplitude with increasing number of transfer cycles. The charge transfer losses are therefore negligible.

Summary of chapter 10

The simulation results were experimentally verified by injecting signal charges in the pnCCD pixels with a laser setup and observing the charge spilling into the neighboring pixels. Optimizing the operating conditions and space charge distributions according to the results of the 2D numerical device simulations, leads to a charge handling capacity of approximately 2.8×10^6 electrons in CCD 2. However, due to limitations of the readout electronics the electron signal in the pixels is cut at lower values.

11 Analytical model of the charge handling capacity

In this chapter, the charge handling capacity is quantitatively related to the operation conditions and the design data of the pnCCD. In this way, the model conception determined from the results of the numerical device simulations is directly connected to the experimental results. The presented model relates the charge handling capacity of a pixel to the electric capacitance of a parallel-plate capacitor [13], [33]. The register contact acts as positive plate, while the negative plate is a virtual plane in the silicon bulk at the storage depth of the signal electrons. The capacitance C of a parallel-plate capacitor consisting of two parallel plates of an area A, which are separated by a distance d, is given by:

$$C = \varepsilon_0 \cdot \varepsilon_{Si} \cdot \frac{A}{d} \tag{11.1}$$

with ε_0 being the vacuum permittivity and ε_{Si} the relative static permittivity of silicon. The pixel size and therefore the area A, under which the electrons are stored, is fixed. So, a reduction of the storage depth, here denoted as distance d, increases the charge handling capacity. The storage depth corresponds to the depth of the potential minimum for electrons under the register side. In order to calculate the electric potential inside the device, the pnCCD is approximated by a simple pnp-structure depicted in figure 11.1 [29]. The structure consists of a weakly n-doped silicon substrate, which is fully depleted. On both side of the wafer, there are strongly p-doped contacts.

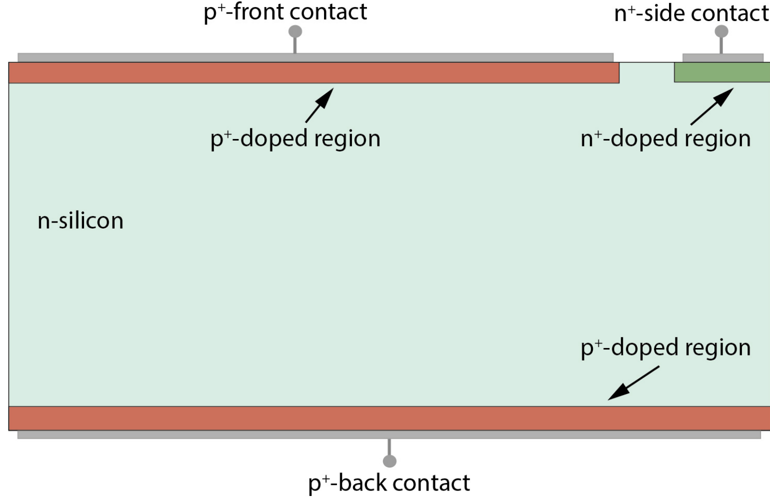

Figure 11.1: Schematic structure of a pnCCD. There are p^{+}-doped contacts on both sides of the weakly n-doped silicon bulk. Since there is a n^{+}-contact on the right side, the structure consists of two pn-junctions, corresponding to the classical sideward depletion scheme. With sufficiently negative p^{+}-contact voltages, the device can be fully depleted.

Additionally, there is a strongly n-doped contact at the front side. The high energy implantation (figure 11.2) is realized by an n-doped layer at the register side. It fixes the storage depth of the signal electrons to a few micrometers below the register side. Actually, the distribution of the high-energy implantation has a peak at a depth of 7 µm, but for reasons of simplification, the ion implantation dose is assumed to spread homogeneously from the register side to a depth of 10 µm. The device is divided into two regions: region 1 reaching from the register side to a depth of 10 µm and region 2 reaching from a depth of 10 µm to 450 µm. The Poisson's equations for region 1 and 2 (figure 11.2) can be expressed as follows:

$$\frac{\partial^2 \varphi_1}{\partial z^2} = -\frac{\rho_1}{\varepsilon_0 \varepsilon_{Si}} \qquad ; \qquad 0 \leq z \leq z_{HE} \tag{11.2}$$

$$\frac{\partial^2 \varphi_2}{\partial z^2} = -\frac{\rho_2}{\varepsilon_0 \varepsilon_{Si}} \qquad ; \qquad z_{HE} \leq z \leq z_b \tag{11.3}$$

$\rho_1 = -e \cdot N_D(1)$ is the space charge distribution of region 1, $\rho_2 = -e \cdot N_D(2)$ is the space charge distribution of region 2, φ_1 und φ_2 are the values for the electric potential in region 1 and 2, z_{HE} is thickness of the high-energy layer and z_b is the thickness of the detector.

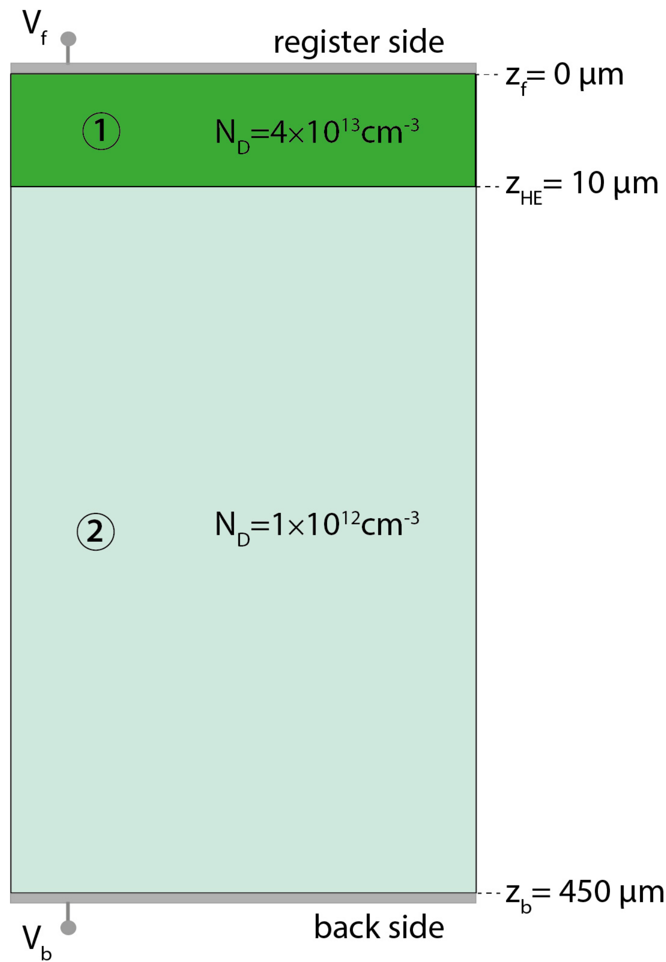

Figure 11.2: Sketch of a pnCCD with high-energy phosphorous implantation layer. The high-energy phosphorous implantation layer is located under the register side of the 450 µm thick silicon substrate. In this simplified model it is assumed, that the donor concentration of the high-energy implantation layer is homogeneously distributed over a 10 µm thick layer.

The following boundary conditions are applied:

$$\varphi_1(z=0) = V_f \quad ; \quad \varphi_2(z=z_b) = V_b \tag{11.4}$$

$$\frac{\partial \varphi_1(z=z_{HE})}{\partial z} = \frac{\partial \varphi_2(z=z_{HE})}{\partial z} \quad ; \quad \varphi_1(z=z_{HE}) = \varphi_2(z=z_{HE}) \tag{11.5}$$

Here, $z = 0$ corresponds the register side and z_b corresponds the back contact. V_f is the voltage applied to the front side und V_b is the voltage of the back contact. The electric potential inside the pnCCD can be described with the following equations. Index 1 is related to the high-energy layer and index 2 to the rest of the substrate.
From equation (11.2)- equation (11.5) follows:

$$\varphi_1(z) = -\frac{\rho_1}{2\varepsilon} \cdot z^2 + \left[\frac{V_b - Vf}{z_b} + \frac{\rho_2}{2\varepsilon} \cdot z_b - \left(\frac{\rho_2}{\varepsilon} - \frac{\rho_1}{\varepsilon} \right) \left(z_{HE} - \frac{z_{HE}^2}{2z_b} \right) \right] \cdot z + V_f \quad (11.6)$$

$$\varphi_2(z) = -\frac{\rho_2}{2\varepsilon} \cdot z^2 + \left[\frac{V_b - Vf}{z_b} + \frac{\rho_2}{2\varepsilon} \cdot z_b - \left(\frac{\rho_2}{\varepsilon} - \frac{\rho_1}{\varepsilon} \right) \frac{z_{HE}^2}{2z_b} \right] \cdot z - \left(\frac{\rho_2}{2\varepsilon} - \frac{\rho_1}{2\varepsilon} \right) \cdot z_{HE}^2 + V_f \quad (11.7)$$

with $\varepsilon = \varepsilon_0 \cdot \varepsilon_{Si}$. The potential minimum und thus the storage depth of the electrons fulfills the condition $\frac{\partial \varphi_1}{\partial z} = 0$. Therefore, the storage depth is:

$$z_{min} = \left[\frac{V_b - Vf}{z_b} + \frac{\rho_2}{2\varepsilon} \cdot z_b - \left(\frac{\rho_2}{\varepsilon} - \frac{\rho_1}{\varepsilon} \right) \left(z_{HE} - \frac{z_{HE}^2}{2z_b} \right) \right] \cdot \frac{\varepsilon}{\rho_1} \quad (11.8)$$

with $z_b = 450\,\mu m$, $z_{HE} = 10\,\mu m$, $\varepsilon = 8.85418 \times 10^{-12} \frac{C}{Vcm} \cdot 11.8 = 1.054 \times 10^{-12} \frac{C}{Vcm}$, $e = 1.602 \times 10^{-19} C$, $N_D(1) = 4 \times 10^{13} cm^{-3}$ and $N_D(2) = 1 \times 10^{12} cm^{-3}$. The concentration of donor ions for pnCCDs with a pixel size of 48 µm × 48 µm and 75 µm × 75 µm is identical. The back contact voltage V_b and the voltage applied at the front side V_f, corresponding to the register offset value, are also identical. In standard operation mode, a back contact voltage V_b = -230 V and a voltage V_f = -18 V of the storage register at the front side is applied. In HCHC-mode, the applied voltages are V_b = -400 V and V_f = -14 V. Thus, in standard operation mode, the potential minimum is at a depth of 7.5 µm and in HCHC-mode at a depth of 1.2 µm under the register side. These values are in good agreement with the results of the two-dimensional numerical device simulations, which are 7 µm in standard operation mode and 1.4 µm for HCHC-mode.

According to the model of the parallel-plate capacitor, the number of electrons, that can be stored in one pixel is:

$$C = \varepsilon_0 \cdot \varepsilon_{Si} \cdot \frac{A}{d} = \frac{Q}{U} \tag{11.9}$$

with $Q = e \cdot N$ the equation is transformed to:

$$N = \frac{\varepsilon_0 \cdot \varepsilon_{Si} \cdot A \cdot U}{e \cdot d} \tag{11.10}$$

Where A is the area under which the signal electrons are stored. Q is the total charge, N is the number of signal electrons and e is the elementary charge. At a certain point in time during a three-phase transfer cycle, the electrons are stored under one register. In this state, the charge density is the highest, and thus the probability that some of the electrons spill into neighboring pixels is at a maximum.
The signal electrons are stored in the area of the highest attraction for electrons, which is the area of the channel notch implants. The channel notches of pnCCDs with a pixel size of 75 µm × 75 µm have an area of 40 µm × 14 µm. For the 48 µm × 48 µm pnCCDs the size of the channel notch is 8 µm × 8 µm. U is the potential barrier between the registers, which is mainly determined by the register amplitude. The influence of the ion implantations on the pixel structure is not taken into account in this simple model. For the pnCCDs with a pixel size of 75 µm × 75 µm, the Φ-amplitude of the register is -9 V in standard operation mode and -12 V in HCHC-mode. For the pnCCDs with a pixel size of 48 µm × 48 µm, the Φ-amplitude of the register is -7 V in standard operation mode and -12 V in HCHC-mode.
The charge handling capacity of pnCCDs with a pixel size of 75 µm × 75 µm is therefore 4.4×10^5 electrons in standard operation mode. The measured pixel full well capacity is 3×10^5 electrons. In HCHC-mode, the charge handling capacity is calculated at 3.6×10^6 electrons using equation (11.10). In this mode, up to 2.8×10^6 electrons are counted in one pixel. With the equations above, the charge handling capacity of a pnCCD with a pixel size of 48 µm × 48 µm is calculated to 3.8×10^4 electrons in standard operation mode. The experimentally determined value is 6×10^4 electrons. In HCHC-mode, the pixel full well capacity is calculated to 3.6×10^5 electrons. With the laser setup 3×10^5 electrons are measured. The charge handling capacities determined from the model are in good agreement with the measured values.
The analytical model presented gives a quantitative relation between the pixel full well capacity, the pixel geometry, the process parameters and the operation parameters of the pnCCD. It confirms the concept of the distribution of the mobile charge carriers

and the electric potential determined from the simulation results.

Summary of chapter 11

An analytical model of the charge handling capacity is established. Therefore, the charge handling capacity of a pixel is related to the electric capacitance of a parallel-plate capacitor. The pixel full well capacity calculated with this model is in good agreement with the simulation and the experimental results.

12 Experimental verification of the pnCCD antiblooming mechanism

12.1 Charge drain in the pixel structure

If the number of signal electrons exceeds the pixel full well capacity, the surplus charges spill into adjacent pixels. Therefore, they have to overcome the lowest potential barrier, which are the channel stops in the row direction. Increasing the potential difference between the register side and the back contact side by applying an extremely negative voltage on the back contact pushes the storage depth of the signal electrons closer to the register side. At the location of the MOS registers between the channel stop implants, the potential barrier to the register side is lowered by applying 0 V or a positive voltage to the MOS registers. The n-channel MOS registers are connected to the bulk contacts of the inner substrate at the sides of the pixel array. The electrons are than drained off to the inner substrate contacts via the thin conducting electron accumulation layer under the MOS registers instead of spilling into neighboring pixels (section 8.2). To study the charge drain characteristics and the linearity of the detector response, the intensity of the laser was increased stepwise while the pnCCD was operated in antiblooming mode.

In figure 12.1, the signal of the center pixel, in which the laser spot is focused, is plotted as a function of the number of photons that hit the detector, as well as the integrated signal over the spot for CCD 1 for storage under two registers. The number of generated signal electrons is proportional to the number of incident photons up to approximately 2.8×10^5 electrons. This corresponds to 93% of the pixel full well capacity in standard operation mode, which is approximately 3×10^5 signal electrons. In this linear region, the maximum deviation from linearity is 1%. Since the maximum voltage swing of the anode of CCD 1 is approximately 6×10^5 electrons (section 13.1), the signal is not limited by the readout electronics.

If more than 3×10^5 electrons are generated, the pixel is saturated. The surplus charges are siphoned off and there is only a minor rise of the signal in the center pixel caused

by changes in the electric potential due to the increasing amount of drained off electrons. There is only a minor charge spilling into the adjacent pixels in the row direction, which results in an increase of the integrated signal. The charge handling capacity in antiblooming mode is significantly smaller than the charge handling capacity in HCHC-mode, because the potential barrier between adjacent pixels is reduced (figure 8.4).
It was experimentally confirmed that a significant charge spilling into the neighboring pixels starts at a laser intensity of approximately 1.06×10^7 signal electrons, corresponding to the same amount of optical photons injected in one pixel. Thus, with a charge handling capacity of approximately 2.8×10^5 electrons (figure 12.1) more than 10^7 electrons can be drained to the n-doped inner substrate contacts at the sides of the pixel array.

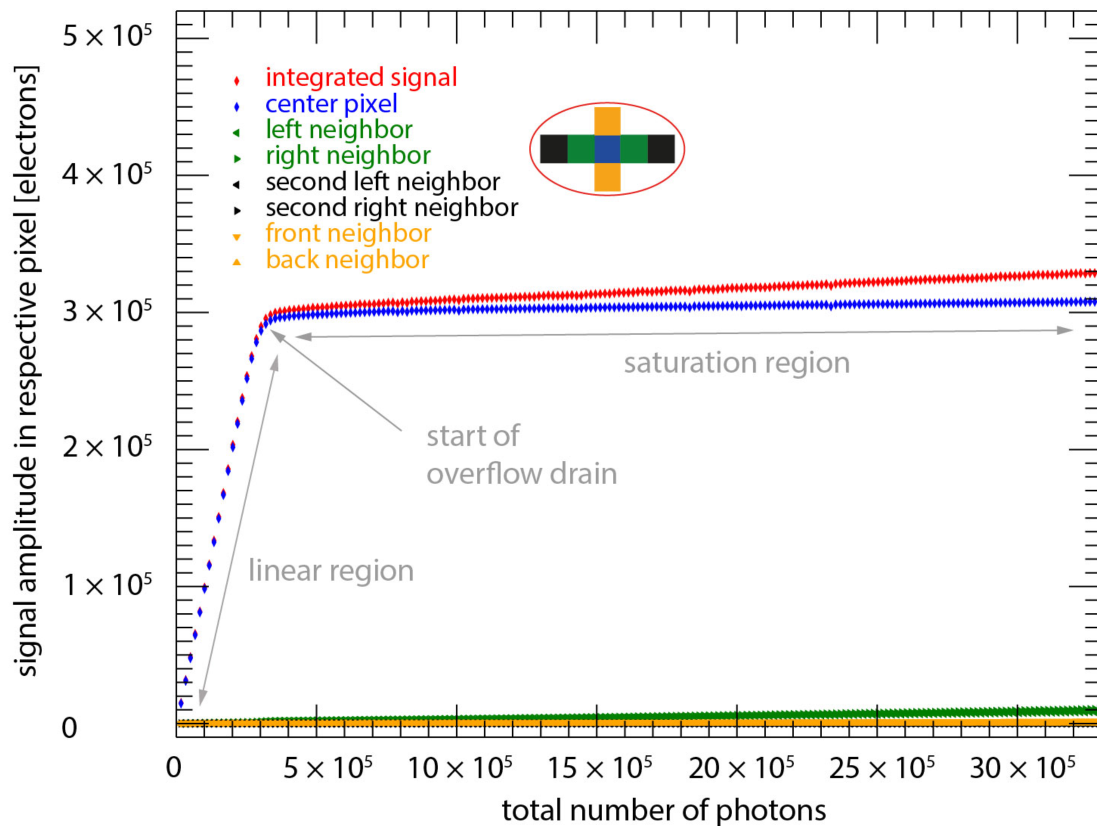

Figure 12.1: Laser linearity measurement in antiblooming mode for storage under two registers. The signal of the center pixel increases with increasing laser pulse width until the maximum charge handling capacity of approximately 3×10^5 electrons is reached. Surplus charges are not spilling into neighboring pixels, but are drained to the inner substrate contacts at the sides of the pixel array via the channel stops and MOS contacts.

If more than 10^7 electrons are injected in one pixel, a significant charge spilling is visible, but most of the excess charges are still removed from the pixel. In total, up to 2.3×10^9 electrons, which is the intensity limit of the laser setup, can be siphoned off one pixel. As the device simulations (section 8.2) have shown, the antiblooming mode is more effective for storage under two registers than for storage under one register. These simulation results were experimentally confirmed (figure 12.2).

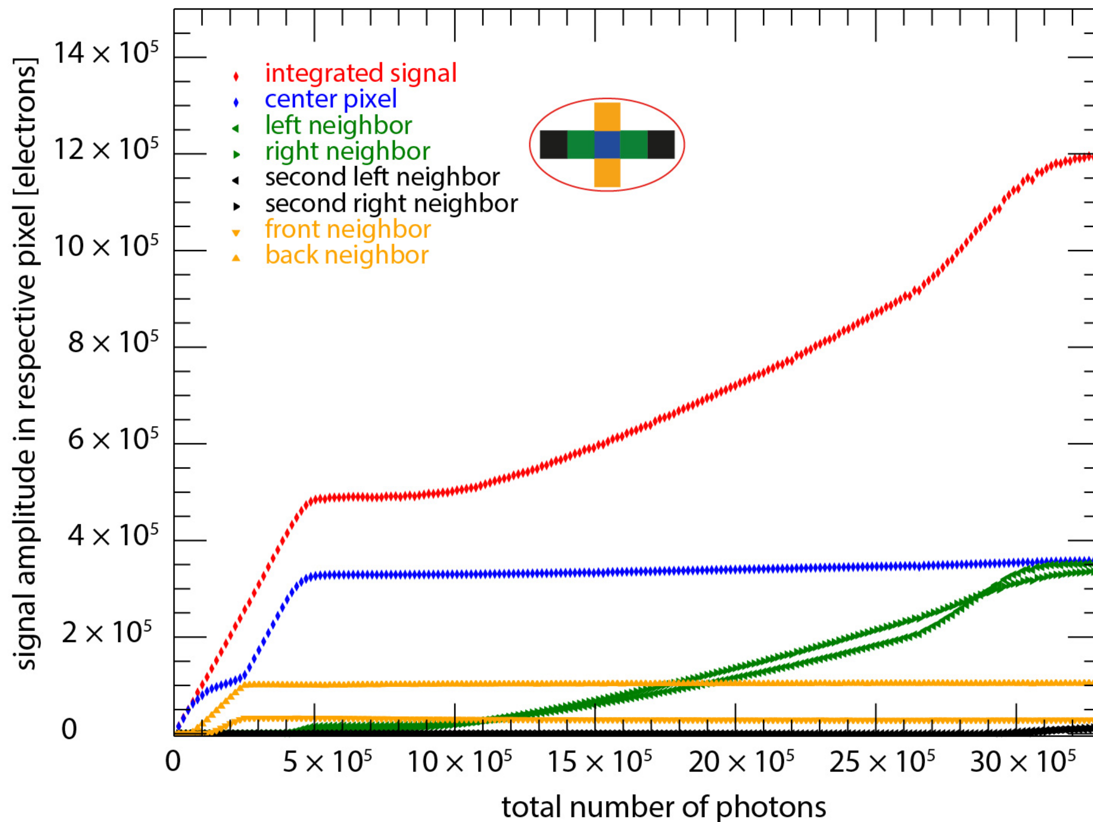

Figure 12.2: Laser linearity measurement in antiblooming mode for storage under one register. As soon as the maximum charge handling capacity is reached, parts of the electrons are drained to the inner substrate contacts at the sides of the pixel array via the channel stops and MOS contacts. The rest of the electrons spill over into the adjacent pixels.

For storage under one register, charge spilling starts at approximately 10^5 signal electrons, although the maximum signal in the center pixel can rise up to 3×10^5 electrons. Due to the positive MOS voltage, the potential barrier in the channel direction is lowered and the signal electrons start to spill over in the channel direction instead of row direction. Parts of the electrons can overcome the potential barrier in the channel direction before the pixel full well capacity is reached. The charge spilling in the row

direction starts for approximately 5×10^5 electrons. The signal in the neighboring pixels in the row direction rises more slowly than in the center pixel, since parts of the charges are siphoned off via the channel stops, while others overcome the channel stops and spill into the adjacent pixels. For storage under one register, the path to the register side is less pronounced and the charge drain mechanism is therefore less effective as for storage under two registers.
For pnCCDs with a pixel size of 48 µm × 48 µm, the number of signal electrons generated in one pixel is preserved up to 1.6×10^5 electrons. As soon as the pixel is saturated, the charge drain effect starts. Approximately one billion electrons can be siphoned off the device before they spill into adjacent pixels. For this type of pnCCD, the charge drain mechanism is also more effective when the signal electrons are stored under two registers during integration time. The simulations showed that, in this case, the potential barrier to the register side is lower, especially in the region of the storage registers (figure 8.4).

12.2 Electric potential profile in antiblooming mode

The electric potential profile in antiblooming mode, especially the position of the charge drain is determined by scanning the pixel structure with the focused laser spot and measuring the amount of drained charges. In figure 12.3, the laser intensity corresponds to approximately 5×10^5 electrons and therefore exceeds the charge handling capacity of approximately 3×10^5 electrons of the antiblooming mode. The laser position scans were performed in the row direction and in the channel direction through the pixel center and the pixel borders. During integration time, the signal charges are stored under two registers. Since the storage area should be in the middle of the pixel, we define that the pixel structure consists of two storage registers (Φ_2 and Φ_3) in the pixel center, which are framed by two half barrier registers (Φ_1).
In figure 12.3A, the scan was performed in the row direction through the middle of the barrier register at the border between two neighboring pixels. When the laser spot scans over the middle of the pixel border, the generated charge cloud spreads equally over both neighboring pixels. The number of signal charges in each pixel is below the maximum charge handling capacity in antiblooming mode and the amount of generated signal electrons is preserved, when the laser spot scans over the channel middle. If the laser spot is moved over the region of charge drain at the channel stops, an increasing number of signal electrons are drained to the n-doped inner substrate contacts at the sides of the pixel array via the MOS structure.

The scan in figure 12.3B is performed through the middle of the pixel in the row direction, which corresponds to the MOS contact in the middle of two storage registers. If the laser spot is located over the channel middle, near the n-implant channel guides and channel notches, the measured amount of signal electrons corresponds to the maximum charge handling capacity of the antiblooming mode, which is approximately 3×10^5 electrons. Any surplus charges are drained to the inner substrate contacts at the sides of the pixel array. If the laser spot is over the channel stops, the amount of signal charges decreases due to charge drain until merely 6×10^4 electrons remain, when the laser spot is directly over the charge drain region. As shown in the simulations, the charge drain is thus stronger in the middle of the pixel between the two storage registers. In the region of the barrier register, approximately 1×10^5 electrons remain when the laser spot hits the channel stop, which is the pixel border in the row direction.
In the channel direction, the pixel structure was also scanned by the laser spot through the pixel borders (figure 12.3C) and the center of the pixels (figure 12.3D). While scanning over the channel stops in the channel direction (figure 12.3C), the signal charges spread equally over the two neighboring pixels. Thus, the number of signal charges in one pixel is below the maximum charge handling capacity in antiblooming mode. However, the channel stops in the region of the MOS contacts is also a position of increased charge drain. Therefore, charges are partially siphoned off if the laser spot is scanned over this area. Since these two effects counteract, the maximum signal in the region of the pixel border in the channel direction decreases, whereas the integrated signal increases. In the pixel middle over the MOS contacts between two storage registers, the charge drain is maximal and the integrated signal is only slightly higher than the maximum signal.
When the laser spot scans over the pixel center in the channel direction, where the channel notch and channel guide implants are located, the signal electrons remain within the pixel (figure 12.3D). The number of electrons in one pixel is limited to the charge handling capacity of the antiblooming mode. Any surplus charges are siphoned off. The pixel border in the channel direction is defined as the center of the barrier register between two adjacent pixels. While moving the laser spot over the pixel border in the channel direction at the location the pixel center, the signal charges spread over the two adjacent pixels according to the position of the laser spot relative to the pixel border. If the laser spot is in the middle of two pixels, the signal electrons spread equally over both pixels. The number of electrons in each pixel is then below the pixel full well capacity in antiblooming mode and the total number of electrons is preserved.

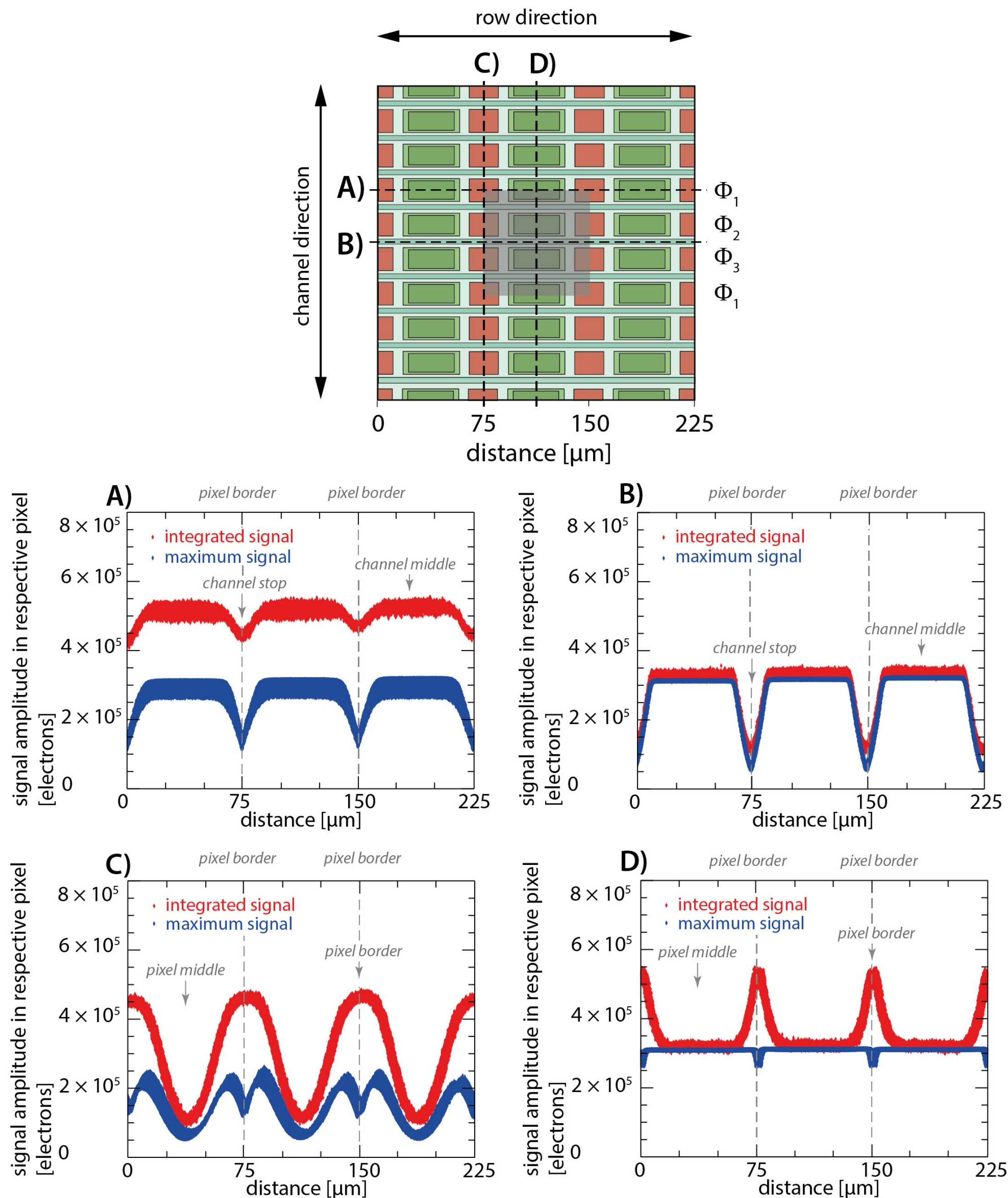

Figure 12.3: Scan over the pixel structure with a focused laser spot in two dimensions. The laser spot scans over the pixel structure in 2 µm steps while operating the pnCCD in antiblooming mode. In A) the pixel structure is scanned over the pixel border in the row direction, which is the middle of the barrier register. In B) it is scanned over the center of the pixel in the row direction, which is the middle of the MOS contact between two storage registers. In C) it is scanned over the channel stops in the channel direction and in D) over the middle of the pixel, in which the channel notch and channel guide implants are located. If the laser scans over the regions of the charge drain, the signal is lower than in the center of the pixel, where the charges are preserved until the maximum pixel full well capacity of approximately 3×10^5 electrons is reached. While scanning over the pixel borders, the charge cloud splits over the neighboring pixels.

Scanning the pixel structure with a laser spot showed that not only excess charges spilling over the pixel border in the row direction are drained off the device but any charges reaching the area of the channel stop and MOS contact. Since signal electrons of charge clouds that split over the pixel border in the row direction are partially drained off, the energy resolution of pnCCDs in antiblooming mode is deteriorated (section 14.2).

12.3 Variation of the pixel charge drain level

The charge drain level of the pnCCD pixels can be adjusted with the operation voltages, especially the MOS voltage and the back contact voltage. The more positive the MOS voltage and the more negative the back contact voltage is, the more effective the pnCCD charge drain mechanism is. Associated with this, the potential barrier between adjacent pixels is lowered, resulting in a lower pixel full well capacity. The charge drain starts at a lower number of electrons in the pixel and a greater number of electrons can be siphoned off the device before charge spilling into neighboring pixels. The potential barrier and thus the charge handling capacity can be increased with a more negative MOS voltage. However, a more negative MOS voltage also increases the potential barrier to the register side, so that the charge drain mechanism becomes less effective. A more positive back contact voltage has the same effect. By varying the MOS voltage and the back contact voltage, the drain level and the efficiency of the charge drain mechanism can be adjusted for the needs of the experiment. This operation mode is called the hybrid operation mode.

Summary of chapter 12

The antiblooming mechanism and the location of the charge drains in the pixel structure was experimentally verified by injecting different amounts of signal electrons in one pixel and scanning over the pixel array with a focused laser spot. It was also shown that the charge drain level can be adjusted with the operation voltages according to the needs of the experiment.

13 Dynamic range of the on-chip electronics

13.1 Limitations of the on-chip electronics

At the end of each channel, the signal charges are shifted to the readout anode, which is connected to a monolithically integrated JFET, the first FET. Integrating the first FET on the chip reduces the effective capacitance of the first amplification stage resulting in a high signal-to-noise ratio. Signal electrons, which are shifted to the last p^+-register, drift to the readout anode, which forms a local potential minimum for electrons. The readout anode is insulated from the other pnCCD contacts and thus acts as capacitor, which is charged by the signal electrons. Since the gate of the first FET is connected to the readout anode, the effective capacitance of the readout anode is the sum of the anode capacitance and the capacitance of the first FET gate, as well as the capacitance of the electrical connections between readout anode and first FET gate. The signal amplitude is proportional to the number of signal electrons shifted on the readout anode. So far, pnCCDs have mainly been used for spectroscopic applications, in which only small amounts of signal charges are detected. Therefore, the capacitance of the readout anode has been kept small to maximize the voltage swing at the first FET in order to obtain a good signal-to-noise ratio for small amounts of signal charges.
For high amounts of signal electrons, the potential difference caused by the signal charges on the anode exceeds the maximum voltage swing that can be processed by the first FET. The signal is cut at the maximum voltage swing of the first FET, which is the threshold voltage of the JFET, although more signal electrons are stored in the pixel. In the studied case, the amount of electrons that can be processed by the on-chip electronics is lower than the pixel full well capacity.
The capacitance of the readout anode, including the first FET gate, is approximately 40 fF $\pm$ (5-8)%. Variations in the capacitance of the readout anode occur because of the production process and lead to different amplification factors of the different pnCCD channels. In addition, the implantation parameters of CCD 1 and CCD 2 and therefore

the threshold voltages differ.
The threshold voltage of the first FETs was determined with test structures located on the silicon wafers of the two pnCCD fabrications that have been studied in this work. The test structures have therefore passed through the same fabrication steps as the pnCCDs. The threshold voltage of the pnCCD first FETs of the studied pnCCDs reaches from 2.5 V to 3.1 V. The maximum voltage swing on the readout anode, which has an electric capacitance of 40 fF, is therefore approximately 5×10^5 - 8×10^5 electrons. Figure 13.1 shows the input characteristic of a pnCCD first FET. The input characteristics of the first FET are measured with test structures containing the identical on-chip electronics of the pnCCD. Signal electrons exceeding this value can not be processed by the readout electronics.

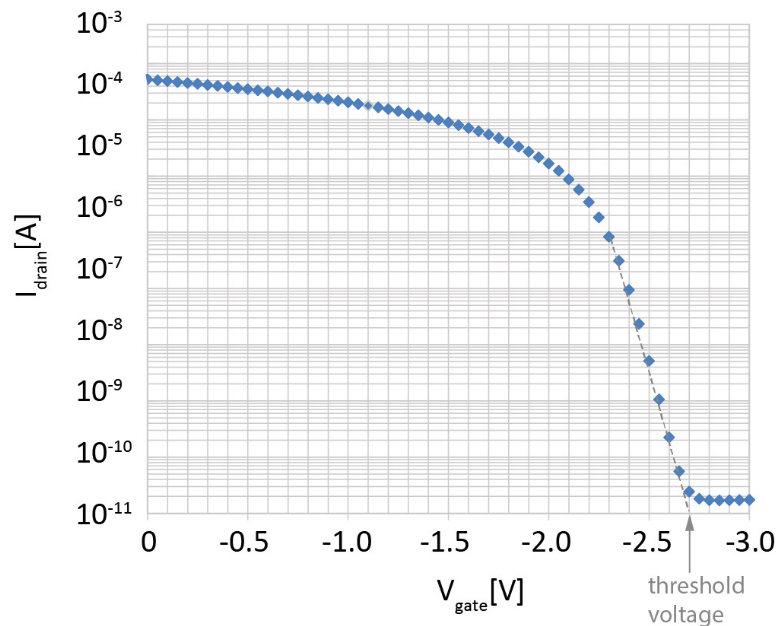

Figure 13.1: Input characteristics of the pnCCD first FET. The first FET acts as first amplification stage on the pnCCD. Its threshold voltage is 2.7 V for CCD 1. The maximum voltage swing on the readout anode is therefore approximately 7×10^5 electrons.

In figure 10.6, the laser intensity was increased in equidistant steps to approximately 1.7×10^7 electrons and the signal of the illuminated pixel and its neighbors was plotted. The data in figure 10.6 are not gain corrected. The signal of the center pixel increases linearely with the laser intensisty until a value of 7.3×10^5 electrons. Although the laser intensity is further increased, there is no charge spilling into neighboring pixels until a laser intensity that corresponds to 2.8×10^6 signal electrons is reached. The signal

amplitude is cut at the threshold voltage of the transistor.
Since the lengths of the electrical connections differ between channels with even and odd numbers, the capacitance of the readout node and therefore the amplification factor is also different. For this reason, the signal of the pixels adjacent to the center pixel is cut at approximately 5.4×10^5 electrons, whereas the maximum signal of the second neighbors is again 7.3×10^5 electrons (figure 10.6).
The dynamic range of the pnCCD is therefore limited by the pixel full well capacity and by the dynamic range of the readout electronics, determined by the threshold voltage of the first FET.

13.2 Enhancing the dynamic range of the on-chip electronics

In order to enhance the dynamic range of the readout electronics, the capacitance of the readout anode was increased. A higher anode capacitance translates a certain amount of charge into a smaller voltage swing. Thus, a higher amount of signal electrons is necessary to produce a voltage swing that corresponds to the limit of the transistor input. However, the signal-to-noise ratio degrades, since for a small number of signal electrons, the difference between the signal and the noise decreases. This effect only plays a role for low intensity experiments and is negligible for high intensity experiments.
In order to increase the capacitance of the readout anode an additional aluminum area was integrated into the pnCCD layout. The capacitance of the readout anode of the channels of CCD 3 is approximately 80 fF and thus twice the capacitance of the readout anodes of CCD 1. Apart from the different capacitances of the anodes, the two pnCCDs are identical.
In figure 13.2, the laser intensity was increased until approximately 1.1×10^6 signal electrons are generated in the center pixel. In CCD 1, the signal amplitude is cut at approximately 5×10^5 signal electrons, whereas in CCD 3 it increases linearely with the amount of generated signal electrons. With the increased anode capacitance, the amount of signal electrons that can be processed by the on-chip electronics was increased by a factor of two. The linearity of the detector response is preserved up to 1.1×10^6 signal electrons. A certain amount of signal charges translates now into a smaller voltage swing of the first FET gates. This also affects the spectrocopic performance of the pnCCD. The noise using a linewise reset increased from approximately 4 electrons (RMS) to approximately 6 electrons (RMS). As the amplification was reduced by a factor of two, the position of the $\mathrm{Mn\,K_\alpha}$ peak is now at approximately 3500 ADU for

CCD 3 instead of approximately 7000 ADU for CCD 1.
In future fabrications, the transconductance of the first FET will be increased to further increase the dynamic range of the pnCCD on-chip electronics.

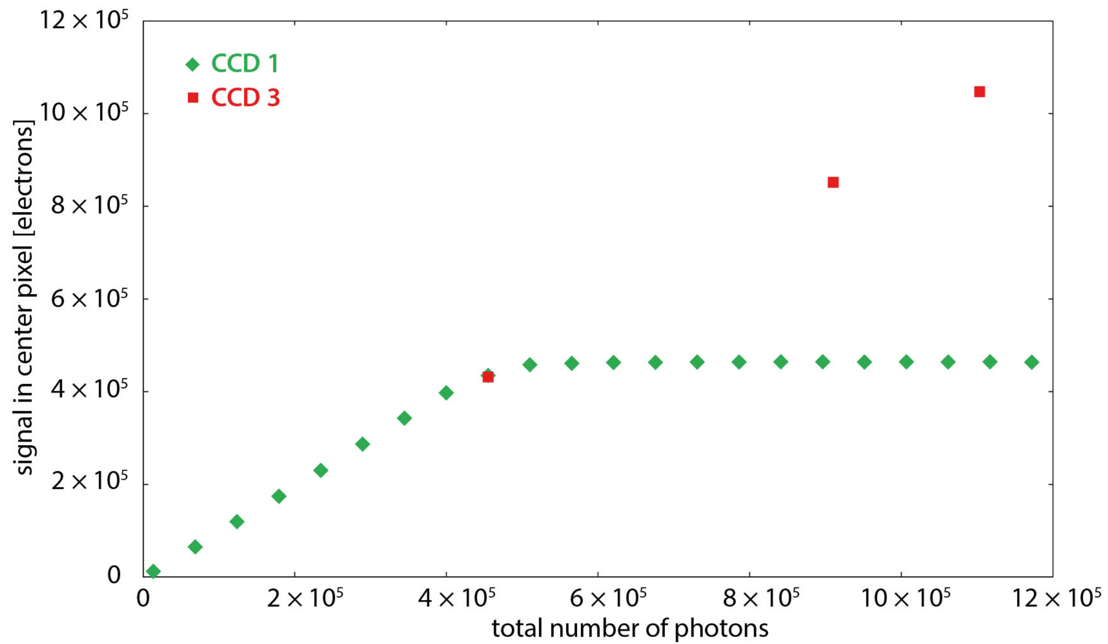

Figure 13.2: Laser linearity measurements with pnCCDs with different capacitances of the readout anode. By increasing the capacitance of the readout anode of CCD 3 compared to CCD 1, the maximum swing of the JFET is increased and the dynamic range of the readout is improved. Therefore, the maximum signal of the laser linearity scan is improved, although the charge handling capacity of the pixels stays constant.

Summary of chapter 13

The amount of signal electrons, that can be processed by the on-chip electronics is limited by the maximum voltage swing of the first FET. For pnCCDs with a pixel size 75 µm × 75 µm it is lower than the pixel full well capacity in high charge handling capacity mode. The dynamic range of the on-chip electronics was increased by increasing the electric capacitance of the readout anode.
A summary of the the main parameters of the different operation modes applied to the pnCCDs tested is summarized in table 13.1.

	start of charge spilling [electrons] in			
	standard mode	**HCHC-mode**	**AB-mode**	**limit of JFET** [electrons]
CCD 1	3×10^5	1.8×10^6	10^7	5×10^5
CCD 2	3×10^5	2.8×10^6	10^7	5×10^5
CCD 3	3×10^5	1.8×10^6	10^7	1.1×10^6
CCD 4	6×10^4	3×10^5	10^7	5×10^5

Table 13.1: Comparison of different pnCCD operation modes. In standard operation mode and HCHC-mode, the charge spilling starts when the maximum charge handling capacity is reached. In antiblooming mode (AB-mode), surplus charges exceeding the maximum pixel full well capacity in this mode are siphoned off the device. Therefore, the charge spilling into neighboring pixels starts at much higher amounts of signal electrons. Because of the limited swing of the on-chip JFET, the measureable electron signal in one pixel is constrained to values below the maximum pixel full well capacity.

14 Spectrocopic properties

The HCHC-mode and the antiblooming mode are used for processing high amounts of signal electrons. Since the electric field in the pnCCD is modified compared to the standard operation mode, the spectrocopic properties of the pnCCD are influenced by the applied voltages.

14.1 Spectroscopic properties of HCHC-mode

For the HCHC-mode, the register voltages and MOS voltage are modified in order to increase the potential barrier between two pixels and therefore the number of electrons that can be stored in one pixel. In standard operation mode, the electric potential profile is kept flat in order to avoid charge generation and thus to be able to detect single photons. A more pronounced electric potential profile induces charge generation at the locations where the p-implants of the transfer registers and the electron accumulation layer below the oxide layer of the MOS gates adjoin each other. At this surface region, the electric field strength is particularely high, increasing the detector noise. The detector noise, using a row-wise reset, a full frame readout speed of 20 Hz and a temperature of -50 °C, is approximately 4 electrons (RMS) in standard operation mode and approximately 4.5 electrons (RMS) in HCHC-mode. During the row-wise reset, the collected signal charges are removed from the readout anode with a reset pulse applied after the readout of each row. During the row-wise reset, it is possible to measure higher amounts of signal charges than during the frame-wise reset, in which the reset pulse is applied after the readout of each frame. Therefore, with frame-wise reset, the amount of signal electrons in one pnCCD channel is summed up on the readout anode during one readout frame, which can lead to saturation of the readout electronics if too many electrons are collected in one channel.
Furthermore, the back contact voltage is set to more negative values, which leads to a steeper potential gradient between front and back side of the device. This results in a shift of the potential minimum closer to the register side, which also increases the charge handling capacity. In addition, a more negative back contact voltage decreases

the time during which the signal electrons need to drift from their generation coordinates to the potential minimum at the register side. Each photon generates a lateral Gaussian distribution of signal electrons, the charge cloud. If the charge cloud extends over pixel borders, the signal electrons are collected in more than one pixel and cause so-called split events.

During their drift in the silicon bulk, the charge cloud expands due to diffusion and electrostatic repulsion of the electrons. The maximum expansion due to electrostatic repulsion takes place immediately after the creation of the charge cloud. At this point, the charges have a very small distance from each other and the repulsive forces are maximal. Afterwards, the expansion of the charge cloud is dominated by diffusion. If the drift time is reduced, the time during which the repulsive forces can act is reduced as well, and the electron cloud expands less than during standard operation. A smaller charge cloud increases the number of single events (i.e., events collected in one pixel).

The reverse effect is utilized for sub-pixel resolution measurements [40]. Here, the back contact voltage is set to a more positive value, to expand the charge cloud and to create more split events. By applying the center of mass method, the photon conversion location can be calculated with an accuracy of less than the pixel size [41].

In figure 14.1, the spectrum of a ^{55}Fe source measured in standard operation mode is shown. In the Mn K_α and Mn K_β peaks, the number of single events is significantly smaller than the number of split events. The same spectrum is measured in HCHC-mode (figure 14.2). Here, single events are the most common type of event, whereas the number of quadruples, which are events that split over four pixels, is significantly reduced.

During event recombination in data analysis, the signal amplitudes of the pixels belonging to one event are summed up. Thus, the noise values of the respective pixels are also added together, which degrades the full width at half maximum of the energy resolution. Since, for single events, only the noise value of one pixel contributes to the full width at half maximum, they have a better energy resolution than spilt events. The energy resolution in HCHC-mode, using a row-wise reset, is 160 eV at full width at half maximum for Mn K_α for all events. The energy resolution is therefore poorer than the full width at half maximum in standard operation mode, which is 170 eV, although the detector noise is slightly higher. The reason is that the amount of single events is more than doubled. Since a single event only has the noise contribution of one pixel, the full width at half maximum is lower than for other events. Increasing the amount of single events due to a reduced charge cloud expansion therefore decreases the full width at half maximum in HCHC-mode.

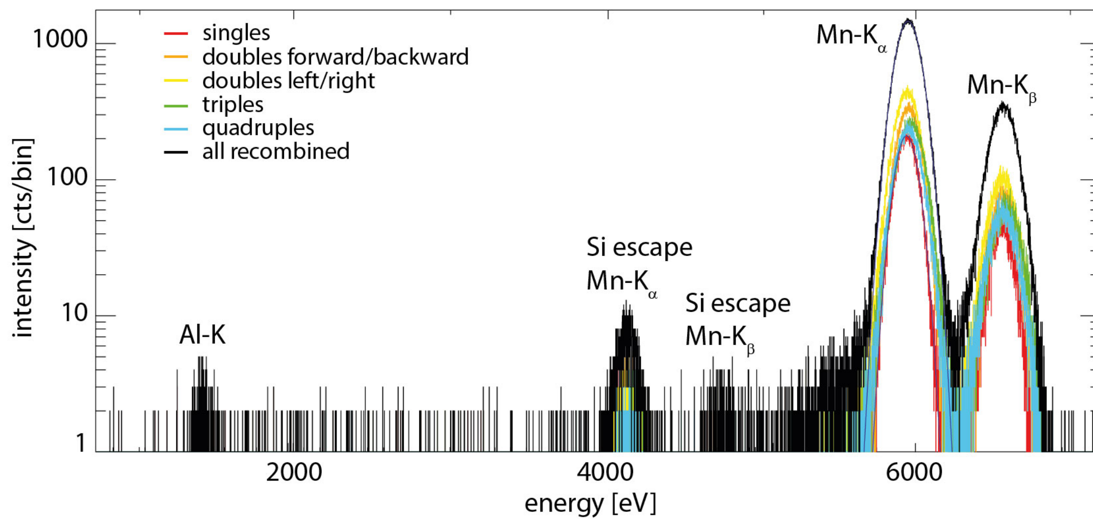

Figure 14.1: Spectral performance in standard operation mode. The spectrum of a $^{55}\mathrm{Fe}$ source was taken in standard operation mode used for spectroscopy. The spectra of the different event types are plotted for the same energy range. Due to the expansion of the charge cloud, the amount of split events is high. In addition to the escape peaks of the $\mathrm{Mn\,K_\alpha}$ and $\mathrm{Mn\,K_\beta}$ lines, a small Al-K peak is observed in the spectrum. It is caused by fluorescence radiation excited by the $\mathrm{Mn\,K_\alpha}$ and $\mathrm{Mn\,K_\beta}$ photons of the radioactive source housing.

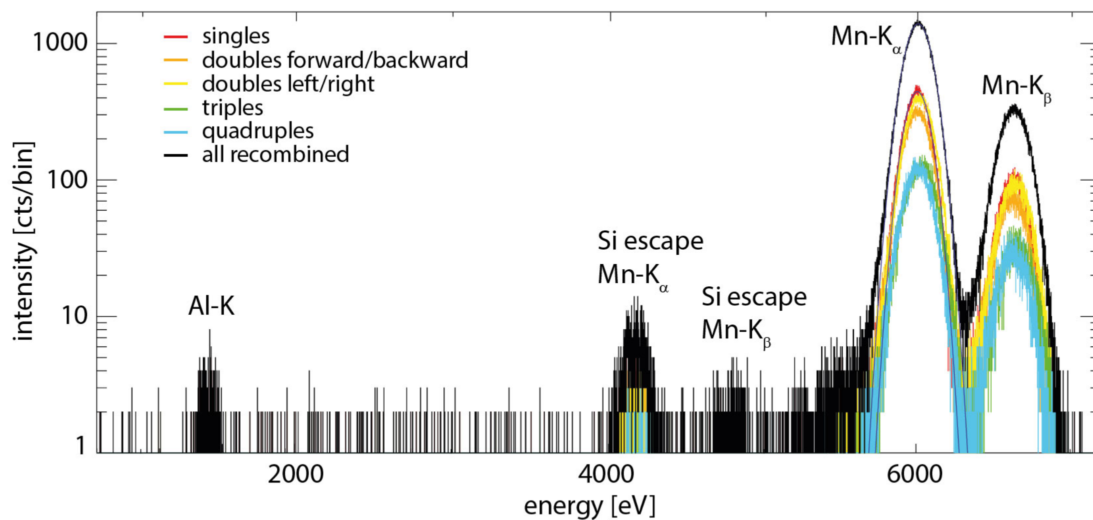

Figure 14.2: Spectral performance in HCHC-mode. The spectrum of a $^{55}\mathrm{Fe}$ source was taken in HCHC-mode. Due to the smaller drift time in HCHC-mode compared to standard operation mode, the amount of single events increases.

14.2 pnCCD performance in antiblooming mode

In antiblooming mode, the negative back contact voltage in combination with a positive MOS voltage creates charge drains at the region of the channel stops and MOS contacts. Charges reaching the pixel borders at the region of the channel stops, which are the pixel borders in the row direction, are partially drained to the inner substrate (section 12.2). In spectroscopic measurements, the charge drain mechanism reduces the number of signal electrons, which are assigned to the photon event that splits over the pixel border. Since the energy of an X-ray photon is proportional to the number of generated signal electrons, the photon events, whose charge clouds spread over the region of the charge drain, are related to photons with lower energies than they actually have.
Figure 14.3 shows a spectrum of a radioactive ^{55}Fe source measured in antiblooming mode. In high charge handling capacity mode (figure 14.2), the Mn K_α peak at 5898 eV has a Gaussian shape and a full with at half maximum comparable to the one in standard operation mode (figure 14.1).

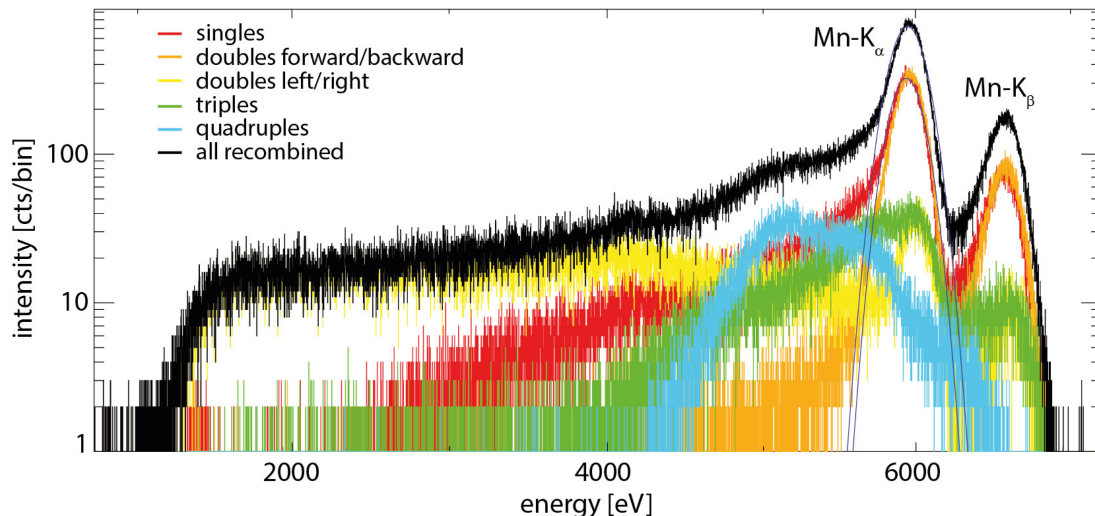

Figure 14.3: Spectral performance in antiblooming mode. The spectrum of a ^{55}Fe source was taken in antiblooming mode. Since singles and doubles forward/backward do not split over channel stops, those events do not lose signal charges and are not broadened to lower energies.

However, in antiblooming mode, the Mn K_α peak has a shoulder at lower energies, especially for split events that expand over the channel stops. Quadruples are particularely affected by the peak broadening, because they split over the regions of the charge drain. Since single events and double forward/backward events do not split over channel stops, these events broaden less to lower energies. The broadening of the peaks of events, that

split over the pixel border in the row direction, confirms that the charges are drained off at the region of the channel stops in antiblooming mode.
Since the signal electrons belonging to one event are partially drained of in antiblooming mode, if the signal cloud splits over the location of the charge drains, this operation mode is not suitable for spectroscopic measurements. However, it can be used as counting mode by integrating over all events of the broaded spectrum. The escape and fluorescence peak, which are overlapped by the broadened peak shoulder, can be neglected. The resulting error is less than one percent.
In order to obtain a precise spatial and intensity information at high intensity diffraction experiments, the measurements have to be performed in both antiblooming mode and HCHC-mode, since the intensity information and the spectrocopic information in antiblooming mode are lost, although the spatial information is preserved event at extremely high amounts of signal electrons.

Summary of chapter 14

In HCHC-mode the spectrocopic performance is comparable to standard operation mode. In antiblooming mode, the spectroscopic information degrades since the signal electrons belonging to an event are partially removed from the device by the charge drains in the electric potential. But the antiblooming mode can be used as counting mode. Combining the information gained from the antiblooming mode and the HCHC-mode provides all information, which are necessary for image reconstruction in diffraction events.

15 Application examples for enhanced dynamic range of the pnCCD

The HCHC-mode and the antiblooming mode are used in experiments, in which extremely high amounts of signal electrons are produced and in which the spatial information is essential for data analysis. Examples are diffraction experiments at FELs and imaging with high energy electrons with electron microscopes.

15.1 Imaging experiments at free electron lasers

pnCCDs with a pixel size of 75 µm × 75 µm are used as imaging spectrometers at free electron lasers. Due to the short wavelength of the FELs and the pulsed structure of the X-ray flashes, it is possible to decipher the structure of biomolecules. For this purpose, the probe particles in solution are injected into the X-ray beam path and the diffraction pattern of each particle hit by an X-ray pulse is recorded by the pnCCD detector. Since the particles are hit in different orientations, the structure of the sample can be reconstructed from the different diffraction images. Some of the diffraction peaks can be very intense, so that the signal charges spill almost over the whole detector plane. The spatial information of the diffraction peaks, which is needed for the reconstruction of the sample structure, is lost. Figure 15.1B shows the diffraction image of a platinum triangle taken in standard operation mode. Those platinum triangles, deposited on silicon substrate, are used for beam characterization at free electron lasers. The platinum triangles are arranged in an array and have an outer line length of 5 µm and a linewidth of 130 nm (figure 15.1A). With each FEL flash, one of the triangles was destroyed and the next triangle was moved into the beam path. The measurements were performed in a fixed-targed setup. The sample produces extremely high diffraction peaks, so that in standard operation mode, the signal charges smear over large areas of the detector (figure 15.1B).

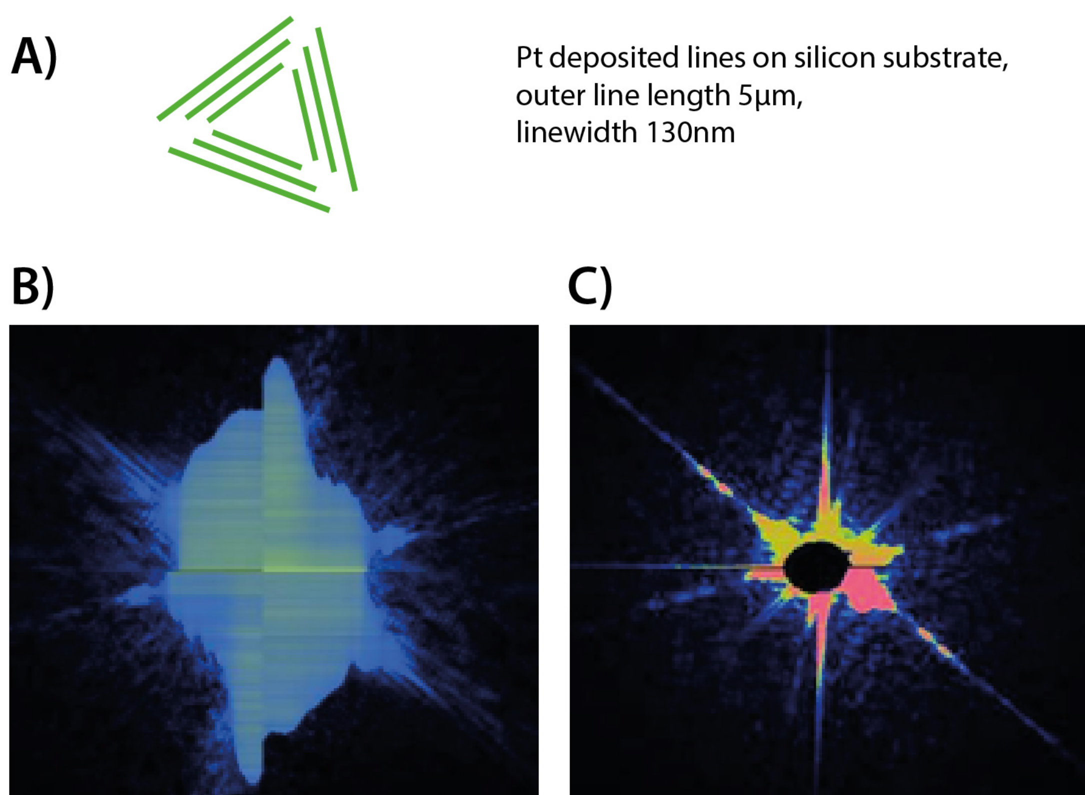

Figure 15.1: Diffraction pattern at FEL with different pnCCD operation modes. A) A silicon substrate with platinum triangles was placed in the beam path of the SLAC-LCLS. B) Diffraction pattern taken in standard operation mode used for spectrocopy. The signal charges are smeared over the area of the diffraction pattern. C) The same scattering process in HCHC-mode. The charge handling capacity is increased and the charge spilling is significantly reduced [42].

The measurements were performed at the Linear Coherent Light Source at the Stanford Linear Accelerator with the CAMP chamber [3] at the Atomic, Molecular and Optical Science (AMO) experimental station during the beamtime of Janos Hajdu from the University of Uppsala in 2013. The CAMP chamber consists of two detector planes with two pnCCDs with 512×1024 pixels of a pixel size of $75\,\mu\text{m} \times 75\,\mu\text{m}$. Figure 15.1B shows the diffraction image in standard operation mode. It was taken by the detector plane which is located closer to the interaction point. The intense direct beam passes through a hole in the detector center (figure 1.1). The pnCCDs used in the CAMP chamber are similar to CCD 1 introduced in section 9.3, but they have a different number of pixels. In standard operation mode, the signal charges spill over large parts of the detector plane and the structure of the diffraction image is lost. In figure 15.1C, an image of the same scattering process was taken in high charge handling capacity mode. In this mode, the charge spilling is significantly reduced and the diffraction pattern is

clearly visible, allowing a reliable image reconstruction. The spatial information and the intensity information of the data are preserved.

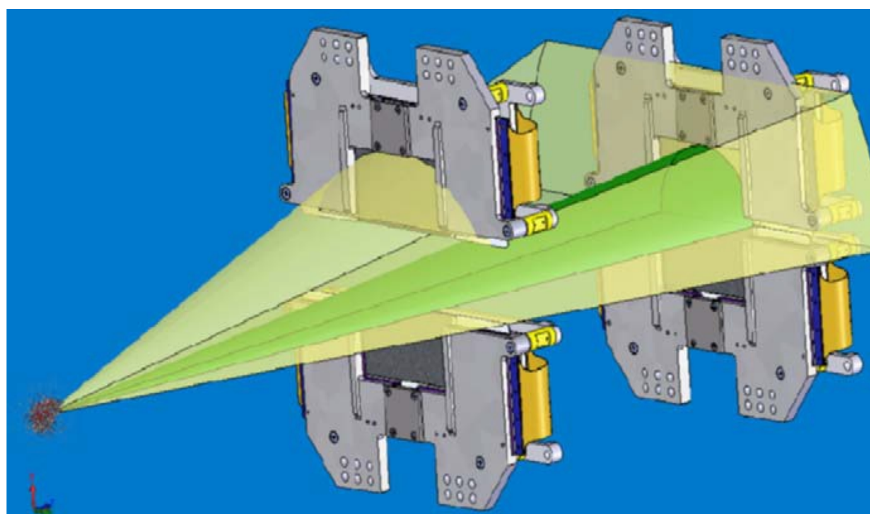

Figure 15.2: Schematic view of the CAMP camera system. The imaging detector system of the CAMP instrument consists of two pnCCD detector planes. The pnCCDs closer to the interaction point detect photons scattered under large angles while the second pnCCD detector plane records X-rays, which are scattered under smaller angles [42].

15.2 Electron diffraction experiments

pnCCDs with a pixel size of 48 µm × 48 µm are used as directly detecting electron imagers for (scanning) transmission electron microscopy ((S)TEM). Scanning transmission electron microscopy is one of the main methods to study materials at the subnanometer scale, including the crystal structures of solids. Because of the short wavelength of the electrons (2 pm- 10 pm), distances smaller than the atomic distances can be resolved [43]. The electron-specimen interaction can provide information on the specimen composition, topography, crystallography, electric potential and local magnetic fields, making the electron microscope a powerful tool for material analysis.

The scanning transmission electron microscope consists of an electron beam generating unit, a system of electromagnetic lenses, scan coils and an imaging system (figure 15.3). The electron source generates electrons either by thermionic or by field emission. The electron beam is accelerated through a high voltage and passes through a system of apertures and electromagnetic lenses to produce a small illuminated spot of about 0.4 nm to 5 nm in diameter. The focused beam scans the specimen by means of scan coils. The

two-dimensional STEM detector is placed below the specimen and collects the electrons scattered from the specimen.
With conventional spatially resolving cameras in electron microscopy, the incoming TEM electrons are converted into optical photons in a scintillator. The optical photons are than imaged with a MOSCCD detector. Through the coupling of the scintillator to a MOSCCD detector the sensitivity and the resolution is reduced [44].

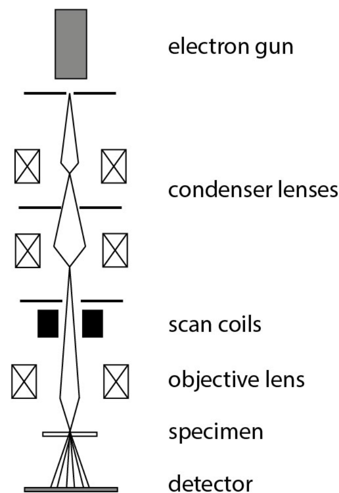

Figure 15.3: STEM principle. The scanning transmission electron microscope can be divided in three essential systems. First, the electron gun producing the electron beam and the condensor system, which focuses the beam onto the specimen. Second, the scan coils which deflect the beam in the x- and y-axes so that it scans over the sample. Third, the image recording system usually consisting of a fluorescent screen and a MOSCCD camera or a CMOS device.

Since pnCCDs are back-illuminated through a thin entrance window and because of their high radiation hardness, it is possible to detect (S)TEM electrons with energies in the range from 300 keV down to 20 keV directly [45]. In a pnCCD, the TEM electrons are scattered in the bulk of the detector, where they create electron-hole pairs (section 2.2). The number of electron-hole pairs depends mainly on the energy of the primary electron. The energy that is required to generate an electron-hole pair in silicon is 3.67 eV. The number of signal electrons that can be stored in one pixel with a size of 48 µm × 48 µm is approximately 6×10^4 in standard operation mode. In the HCHC-mode the pixel full well capacity is approximately 3×10^5 signal electrons (section 13). With a readout rate of 10^3 frames per second (fps) and a TEM electron energy of 80 keV, approximately 1.3×10^4 TEM electrons can be collected in one pixel during 1 s acquisition time. It is assumed that the entire energy is deposited in this pixel.

Due to the enormous contrasts in the experimental data in electron diffraction experiments, the dynamic range of the detector has to be extremely high. For experiments, in which very bright and very weak signals have to be resolved in the same image, the antiblooming mode is the most suitable operation mode.
Figure 15.4 shows an example of a nanobeam electron diffraction pattern taken of a TiFeMo alloy with widely varying intensities of the diffraction peaks. The measurements were performed in collaboration with Duncan Johnstone and Rowan Leary from the University of Cambridge and the Forschungszentrum Jülich.

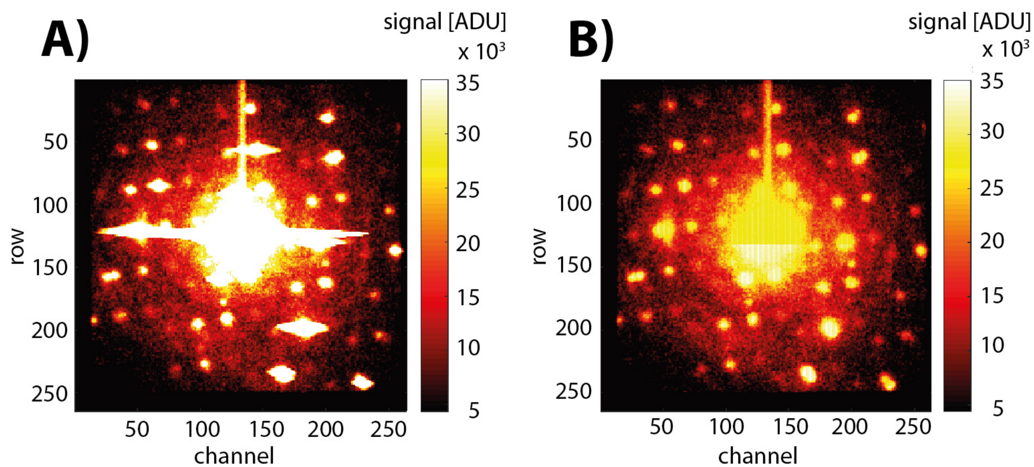

Figure 15.4: Nanobeam electron diffraction of a TiFeMo alloy. The images were taken under the same TEM settings with 200 keV and 10^3 fps. The images are the sum integrated over 50 frames. A) Due to the intense diffraction peaks, the signal charges smear in HCHC-mode in the row direction. B) In antiblooming mode, the excess charges are drained off the device and the locations of the diffraction peaks can be clearly identified [46]. In both images, diffuse scattering around the primary beam and Out-of-Time events are visible.

Nanobeam electron diffraction (NBD) is a technique for qualitative analysis of crystal structures of nanometer areas [47]. A parallel electron beam with nanometer diameter is scanned across the sample producing diffraction patterns with sharp spots for each probe position. From the diffraction pattern, the lattice parameter, lattice type and crystal orientation of the scanned area can be determined.
Because of their high tensile strength, low weight, high corrosion resistance and high temperature stability, titanium alloys are used in many fields, ranging from medicine to aerospace technology. Depending on their composition, TiFeMo alloys consist of different structural phases with different mechanical properties. The aim of the experiment was to analyze the structural phase transitions of an alloy with Ti-40at.%-Fe-20at.%-

Mo-40at.%. In this composition, the TiFeMo alloy forms a superlattice with an ultra-fine lamellar microstructure under appropriate heat treatment [48].
The crystal structure of the TiFeMo is a bcc (body centered cubic) matrix with two different phases (figure 15.5). Mo/Ti forms an A2 phase with a bcc lattice structure with a lattice distance of 3.14 Å. It is strengthened by B2 phase precipates. The B2 phase (TiFe) consists of ordered intermetallic with a lattice distance of 2.84 Å. The solubility between Mo/Ti and between Mo/TiFe offers potential for tailoring lattice misfit to control the mechanical properties of the alloy.

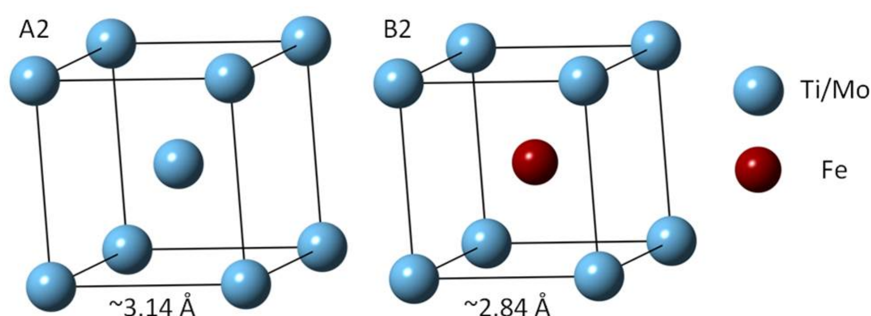

Figure 15.5: Crystal structure of TiFeMo. Crystal structure of the A2 (bcc matrix) and B2 (ordered intermetallic) phases [46].

Since the unit cells of the lamellar structures are periodically arranged in the superlattice, their structure is superimposed by the diffraction pattern of the superlattice [49]. The diffraction peaks in a large distance from the primary beam give the structure of the superlattice and the peaks close to the primary beam determine the lamellar microstructure figure 15.4.
In order to capture the complex crystal structure in a single image, it is important that the diffraction peaks at high angles are properly resolved. Because of the small scattering cross section, the diffraction peaks to be resolved at high angles are weak and need a higher intensity in the primary beam. This results in charge spilling of the diffraction peaks at low angles (which have a higher scattering cross section) even in HCHC-mode (figure 15.4A).
In order to resolve both, the very bright signal of the low angle diffraction peaks and the very weaks signal of the high angle diffraction peaks in the same image, the antiblooming mode was used (figure 15.4B).
Figure 15.6A shows the bright field STEM image of the TiFeMo specimen recorded with 512×512 probe positions. The image was taken in HCHC-mode. When the electron

beam is scanned over the specimen, the electrons are diffracted at the sample and a diffraction image is generated for each probe position. A representative diffraction pattern of the TiFeMo sample is shown in figure 15.6B. The diffraction pattern was taken in antiblooming mode with a readout speed of 10^3 fps.

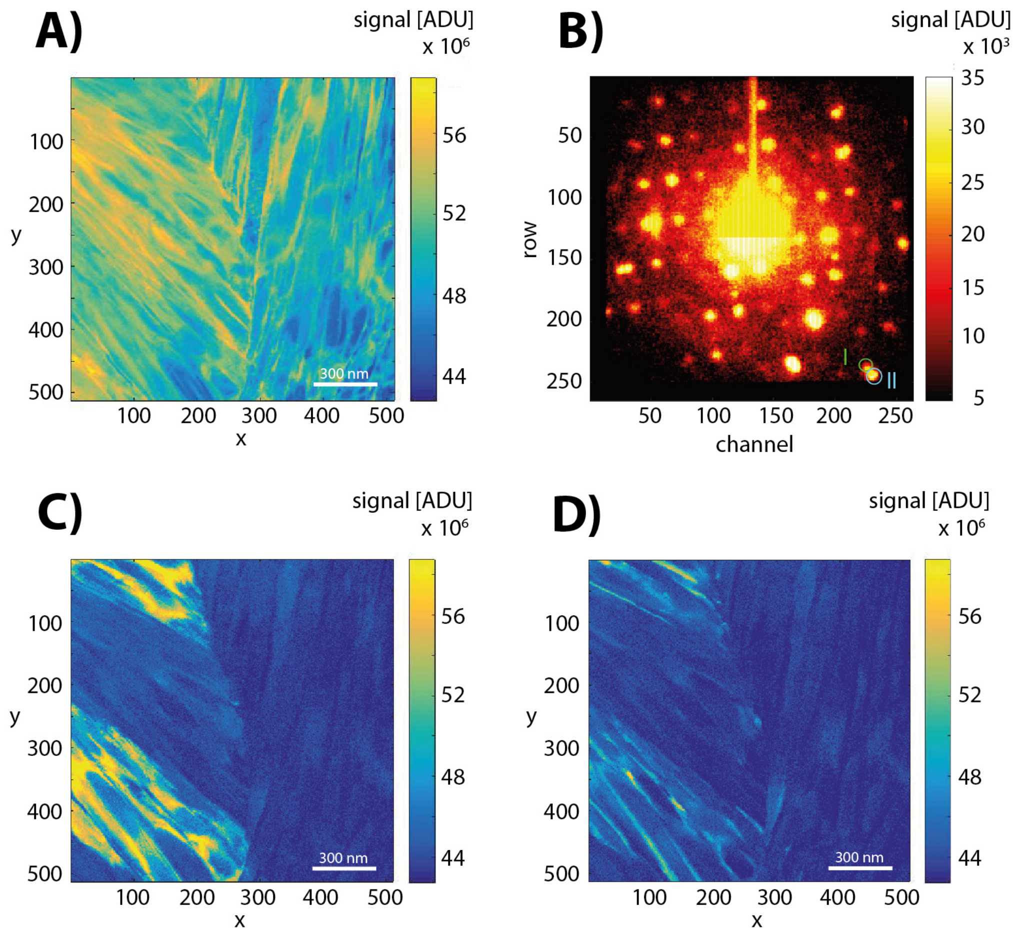

Figure 15.6: Phase identification of TiFeMo A) 512×512 bright field STEM image of TiFeMo recorded in HCHC-mode. Each pixel value is the integrated sum over the full diffraction pattern of the 264×264 pixels of the pnCCD. B) Representative diffraction pattern of TiFeMo recorded in antiblooming mode for a readout speed of 10^3 fps. Virtual diffraction images using the integration windows I and II in the diffraction pattern (lower right in the diffraction pattern) reveals the position of the A2 phase (C) and the B2 phase (D) [46].

Each pixel value of figure 15.6A is the integrated sum over the full diffraction pattern of the pnCCD at the corresponding probe position.

The position of the peaks in figure 15.6B gives the lattice distance of the bcc matrix. According to Bragg‘s law [16], the smaller lattice distance of the B2 phase compared

to the A2 phase causes the diffraction peaks to be shifted to higher angles. The shift of the diffraction peaks in the integration windows I and II in the diffraction pattern (figure 15.6B) reveals the position of the A2 phase and the B2 phase in the specimen. The position of the A2 phase (figure 15.6C) and the B2 phase (figure 15.6D) are marked in yellow in the corresponding virtual diffraction images.
In order to analyze the elemental composition of the specimen on the nanometer scale, energy-dispersive X-ray spectroscopy (EDX) measurements were performed in parallel to the STEM diffraction measurements. In STEM-EDX, the atoms of the specimen are stimulated by the beam electrons to emit characteristic X-rays which have element-specific energies. The X-rays are than detected by an energy dispersive Silicon Drift Detector (SDD) [10].
Figure 15.7 shows a high angle annular dark-field STEM image on the left. The lamellar structure of the specimen is clearly visible. On the right hand side of the image are the elemental maps for Ti, Fe and Mo obtained from the STEM-EDX measurements. To form these elemental maps the intensity in the corresponding K_α X-ray peaks was integrated.

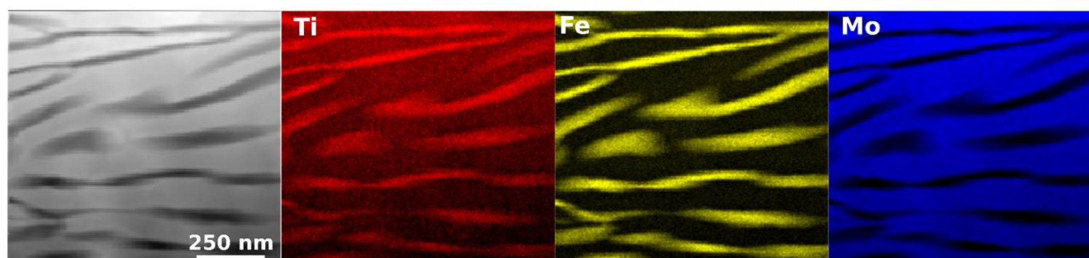

Figure 15.7: STEM images of TiFeMo. High angle annular dark-field STEM image (left) and the elemental maps for Ti, Fe and Mo formed by integrating the intensity in the corresponding K_α X-ray peaks obtained via STEM-EDX [46].

Because of the small thickness of the STEM samples and therefore relatively small ionization volume, the amount of X-ray photons generated from the electron-specimen interaction is small. Furthermore, the EDX-detector is placed at high angles (40°- 60°) [43], so a high intensity electron beam is necessary to produce a sufficient number of X-ray photons for the elemental characterization of the sample. But a high intensity electron beam can lead to charge spilling in the electron detector. Therefore, electron detectors with high dynamic range such as pnCCDs using the HCHC-mode and antiblooming mode are required for those experiments.
Another electron diffraction technique is the so-called convergent beam electron diffrac-

tion (CBED) method [50]. CBED is a technique similar to nanobeam electron diffraction but it substitutes a focused electron beam for the NBD collimated electron beam. The diffraction patterns now form discs. The positions of the diffraction discs are related to lattice plane spacings via Bragg‘s law. The lattice distance and any deviations (e.g., lattice strain) can be determined by the relative shift of the diffraction discs. Compared to NBD, the precision of the strain measurement increases, since the shift can be determined more precisely with disc-shaped diffraction peaks [43]. Furthermore, the spatial resolution increases in CBED, since the diameter of the electron probe decreases.
In figure 15.8, a focused electron probe with a diameter of 0.5 nm was scanned over a semiconductor layer stack with alternating compressive and tensile strain. The diffraction discs were recorded with the pnCCD detector. The specimen consists of an $\mathrm{In_xGa_{1-x}N_yAs_{1-y}}$ layer stack buried in GaAs [51]. Figure 15.8A shows the dark field STEM image of the investigated sample superimposed by the strain profile obtained with a conventional CCD. The electron microscope was operated in STEM mode at 300 keV with a semiconvergence angle of 2.6 mrad of the scanning probe. Figure 15.8B shows the strain profile measured by a pnCCD with an integration time of 200 ms and figure 15.8C with 1 ms integration time. The pnCCD was operated in standard operation mode.
As an example, the results of the 400 reflection in GaAs are presented. According to Bragg’s equation, the position of the 400 diffraction disc changes with the (400) lattice plane spacing in the illuminated volume. Since the semiconvergence angle of the STEM probe is known, the shift of the diffraction disc can be converted to angular changes $\Delta\theta$ by using the radius in pixels obtained by the radial gradient algorithm method [52]. The strain in [100] direction is then given by [51]

$$\varepsilon_{[100]} = \frac{sin\theta_{400}^{B}}{sin(\theta_{400}^{B} + \Delta\theta/2)} - 1 \tag{15.1}$$

with θ_{400}^{B} being the Bragg angle of the 400 reflection in GaAs.
The strain precision obtained from these measurements is 13×10^{-4} for 1 ms acquisition time. As shown in figure 15.8D, there is a large variation in the intensity of the diffraction discs for different scan positions. The signal electrons of the intense diffraction discs must not spill over but at the same time, the intensity of the disc has to be high enough so that the disc can be identified by the disc position recognition algorithm.

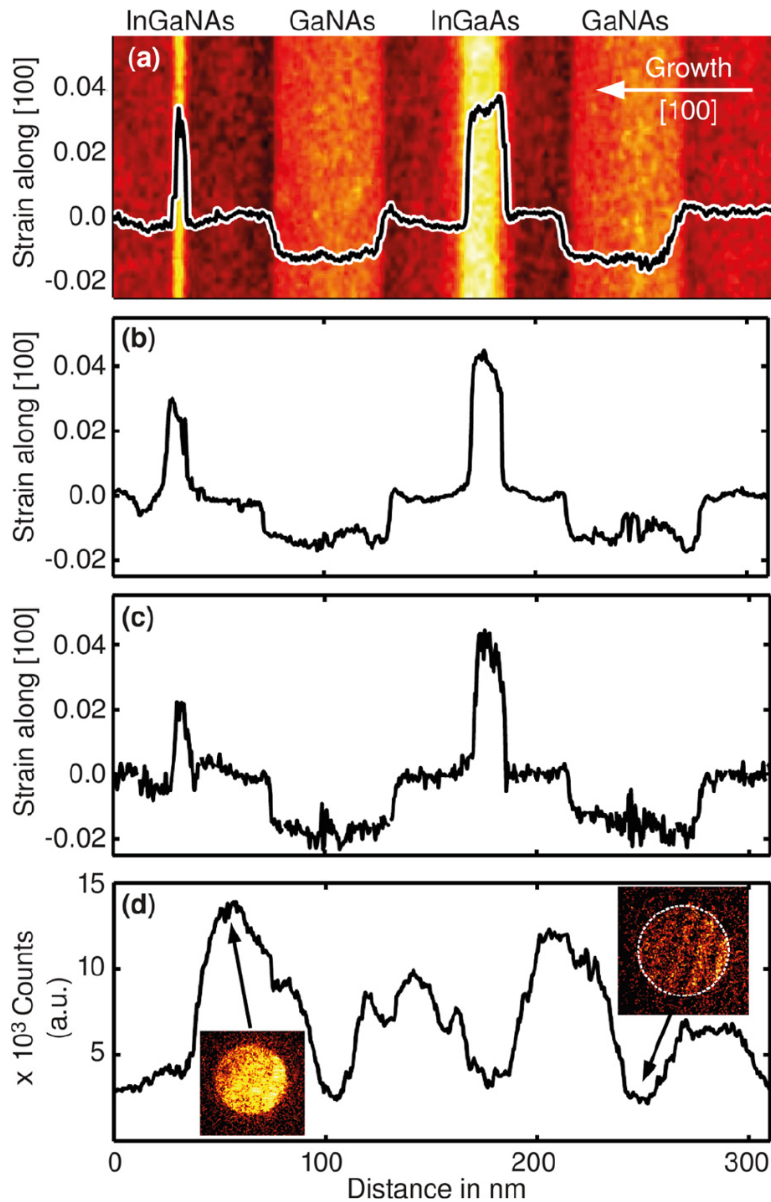

Figure 15.8: Strain measurement in semiconductor herterostructures. A) Dark field STEM image of an $\mathrm{In_xGa_{1-x}N_yAs_{1-y}}$ layer stack buried in GaAs. The strain profile obtained with a conventional CCD using acquisition times of 500 ms is superimposed. With a pnCCD, the strain profiles were measured with integration times of 200 ms (B) and 1 ms (C). D) The counts of a millisecond frame are plotted in dependence of the scan position. The inset images depict examples for high and low excitation of the disc of the 400 reflection. In the latter cases it contains the fitted circle [51].

In order to get enough signal even in the low excitation discs, the primary electron has to be very intense, which then leads to charge spilling in the high excitation discs. This can be prevented by using the HCHC-mode or the antiblooming mode instead of the standard operation mode.
Instead of the beam intensity, the acquisition time can be increased. However, short acquisition times are important to increase the sample throughput and to be able to perform measurements during which the parameters are stable. For longer acquisition times, the sample can drift from heat expansion due to the energetic electron beam or mechanical instabilities. Furthermore, the sample structure is degraded due to carbon depositions from the sample environment. By increasing the acquisition time of a factor of five from 1 ms to 5 ms, the strain precision was increased from 13×10^{-4} to 9.5×10^{-4}. The same effect can be observed by increasing the charge handling capacity of a factor of five compared to standard operation mode without increasing the acquisition time.
However, in most experiments it is not possible to adjust the beam parameter to avoid pixel saturation during the measurements.
An example, in which charge spilling is not avoidable in standard operation mode is presented in the following [53]. Figure 15.9 shows STEM diffraction discs of a MOSFET device. The measurements were performed within a collaboration with Andreas Rosenauer and Knut Müller-Caspary from the University of Bremen. The aim of the experiment was to analyse the strain in the silicon after ion implantation [51] by using convergent beam electron diffraction [54].
In the following example images, the different pnCCD operation modes are compared. Figure 15.9 shows images of STEM diffraction discs of a MOSFET device taken under constant electron microscope settings with 300 keV and 10^3 fps. The same location of the sample was studied in all images of figure 15.9. Figure 15.9A was taken in standard operation mode. As the number of electrons that can be stored in one pixel is limited to approximately 6×10^4 electrons in this mode, blooming is observed and the exact location of the diffraction discs is reduced.
This charge spilling is significantly reduced after switching to the HCHC-mode with a charge handling capacity of approximately 3×10^5 electrons (figure 15.9B). The structure of the STEM diffraction discs appears more defined, but there is still a charge spilling due to saturation in some pixels.
In the antiblooming mode, the structure of the sample is evidently without any charge smearing effects, but the charge handling capacity is reduced to approximately 1.7×10^5 signal electrons (figure 15.9D).

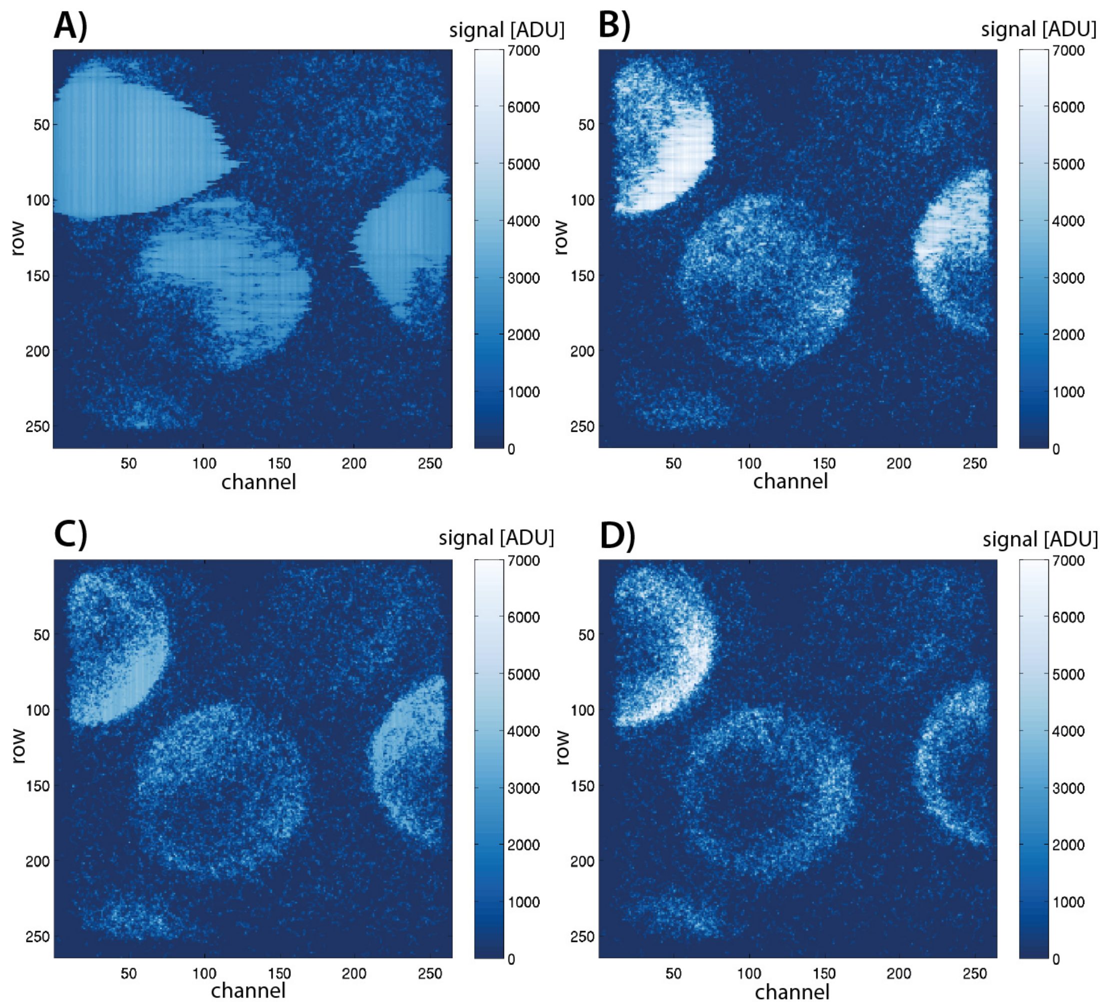

Figure 15.9: STEM diffraction discs of a MOSFET device. The images were taken under the same TEM settings with 300 keV and 10^3 fps. A) Standard operation mode with charge blooming due to the limited number of electrons that can be stored in one pixel. B) HCHC-mode with increased pixel full well capacity, so that a higher number of signal electrons can be stored in one pixel. Due to the extremely high number of signal electrons in this experiment, there is still charge spilling into neighboring pixels. C) In antiblooming mode, any surplus charges are drained to the inner substrate. The structure of the STEM diffraction disc appears defined. D) In the hybrid operation mode, the antiblooming capabilities are limited, but the pixel full well capacity is increased compared to the antiblooming mode [55].

In figure 15.9C, the charge drain level was adjusted with the pnCCD operation voltages as shown in section 12.3. The charge drain now starts at a higher number of electrons, but is therefore also less effective than in antiblooming mode. In this so-called hybrid operation mode the charge handling capacity is with 2.5×10^5 electrons higher than in antiblooming mode, but since the antiblooming capabilities are limited, some spots are

still slightly smeared (figure 15.9C).
Compared to standard operation mode, the dynamic range is significantly enhanced in the new pnCCD operation modes. The signal per readout can be increased or the readout time can be decreased keeping the same signal level.
A higher signal leads to a more precise determination of information about the sample, in this case, the lattice constants or lattice strain. Alternatively, larger fields of view on the sample can be scanned in a shorter timeframe.

Summary of chapter 15

The results of this work were used to develop new pnCCD operation modes which increase the dynamic range of the detector. It was shown that due to the high charge handling capacity mode and the antiblooming mode, the pnCCD can now resolve the large contrasts in X-ray as well as in electron diffraction experiments. Compared to the standard operation mode, the acquisition time can be reduced by a factor of more than five, since the intensity in the primary beam can be increased because of the enhanced dynamic range of the pnCCD, increasing the specimen throughput. Due to the reduction of the acquisition time, now stable measurements can be performed at specimens which degenerate during the experiment.

16 Conclusion

The extremely intense X-ray pulses of the fourth generation synchrotrons (i.e., the free electron lasers) pose considerable challenges to the dynamic range of the detector system. In this study, the dynamic range of the pnCCDs was improved by increasing the charge handling capacity by approximately a factor of ten. Relating the charge handling capacity to an electric capacitance, the number of signal charges that can be stored in one pixel depends on the height of the potential barrier between the potential wells and the storage depth. By using two-dimensional numerical device simulations, the influence of the operation conditions of the pnCCD and the space charge distributions were studied. The experimental confirmation of the simulation results was performed with a laser setup.
The potential barriers in the channel direction can be varied by changing the register voltages and the voltages applied to the MOS contacts. The MOS contacts are located between the p^+-registers at the front side of the device and serve as additional potential barriers between them.
In the row direction, the predominant spilling direction, the potential barriers are formed by channel stops. The negative space charges of the p-implanted channel stops have the same effect as electrodes with a fixed voltage. The higher the ion implantation dose of the channel stops, the more repulsive this region is for electrons. The electric potential difference between the attractive and repulsive parts of the pixel was increased by increasing the ion implantation dose of the n-doped channel guide and channel notch. The increase of the implantation dose of the n-implants makes the pixel center more attractive for electrons. The implantation parameters have to be modified carefully to avoid avalanche like leakage currents because of strong electric fields (bright pixels). In order to shift the storage depth closer to the register side, the back contact voltage was set to a more negative value. A silicon wafer with a higher resistivity due a lower bulk-doping has a lower depletion voltage, which also results in a shift of the potential minimum closer to the register side. By combining these effects, the charge handling capacity was increased from originally approximately 3×10^5 electrons to 2.8×10^6 electrons.

A further increase of the dynamic range was achieved by developing a mechanism for controlled charge extraction. In conventional antiblooming CCDs, the antiblooming feature is built into the chip. In contrast, the antiblooming capability of the pnCCD is activatable by applying the appropriate operation voltages. By adjusting the back contact and MOS voltage, the electric potential profile of the pixel structure now gives electrons the possibility to reach the surface of the register side. Once the pixel is completely filled with electrons, excess charges are drained to the n-doped inner substrate contacts at the sides of the pixel array via the thin conducting charge layer under the MOS contacts. In this way, up to 2.3×10^9 electrons, which is the intensity limit of the laser setup, can be siphoned off one pixel and charge spilling into neighboring pixels is prevented. The antiblooming mechanism preserves the spatial information of the diffraction peaks in diffraction experiment, which is essential for the reconstruction of the probe structure.
But high amounts of signal charges do not only cause charge spilling but also a saturation of the readout electronics. The readout electronics is limited by the maximum voltage swing of the readout anode. The maximum voltage swing and therefore the dynamic range of the on-chip electronics was doubled by increasing the electric capacitance of the readout anode.
The enhancement of the dynamic range of the pnCCDs has lead to a better quality of the data for X-ray diffraction experiments at FELs and for the direct detection of primary electrons at electron microscopes. Based on this study, further improvements of the pnCCD layout and process parameters were implemented in ongoing pnCCD productions.

Acronyms

AB-mode	Antiblooming mode
ADC	Analog Digital Converter
ADU	Arbitary Digital Units
AMO	Atomic, Molecular and Optical Science
ASG	Advanced Study Group
ASIC	Application-Specific Integrated Circuit
bcc	Body Centered Cubic
CAMEX	CMOS Analog Multiplier
CAMP	CFEL ASG Multi-Purpose chamber
CBED	Convergent Beam Electron Diffraction
CCD	Charge-Coupled Device
CDS	Correlated Double Sampling
CFEL	Center of Free Electron Laser
CTE	Charge Transfer Efficiency
CTI	Charge Transfer Inefficiency
EDX	Energy-Dispersive X-ray Spectroscopy
ENC	Equivalent Noise Charge
EUV	Extreme Ultra Violet
FEL	Free Electron Laser
FEM	Finite Element Method
fps	Frames Per Second
FWHM	Full Width at Half Maximum

HCHC-mode	High Charge Handling Capacity mode
IDL	Interactive Data Language
JFET	Junction Field-Effect Transistor
LCLS	Linac Coherent Light Source
MIP	Minimum Ionizing Particles
MOS	Metal-Oxide-Semiconductor
MOSCCD	Metal-Oxide-Semiconductor Charge-Coupled Device
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPE	Max Planck Institute for Extraterrestrical Physics
NBD	Nanobeam Electron Diffraction
pnCCD	Charge-Coupled Device with pn-junction transfer gates
RC filter	Resistor-Capacitor filter
RMS	Root Mean Square
SDD	Silicon Drift Detector
SIMS	Secondary Ion Mass Spectroscopy
SRP	Spreading Resistance Profiling
STEM	Scanning Transmission Electron Microcopy
TEM	Transmission Electron Microcopy
TeSCA	Two-Dimensional Semi-Conductor Analysis Package
SLAC	Stanford Linear Accelerator
UV	Ultra Violet
WIAS	Karl-Weierstraß-Institute for Applied Analysis and Stochastics
ZIF	Zero Insertion Force

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Acknowledgements

Finally, I would like to thank all the people who contributed to the success of this thesis.

- First, I would like to express my gratitude to my advisor Prof. Dr. Lothar Strüder, who provided me with guidance and support throughout my work.

- I would also like to thank Prof. Dr. Ullrich Pietsch for his interest and suggestions, and for being second advisor for this thesis.

- Many thanks to Robert Hartmann and Dr. Martin Huth for their support in all kinds of scientific and technical questions.

- I am grateful to Dr. Martin Simson, Dr. Robert Ritz, Dr. Sebastian Send, Jakob Soltau and Daniel Steigenhöfer for providing their support concerning the experimental measurements.

- I also want to thank Dr. Gerhard Lutz and Dr. Nils Kimmel for the fruitful discussions concerning the device simulations and Dr. Stefan Aschauer for his support concerning the three-dimensional device simulations.

- I thank Peter Holl for many helpful discussions concerning the pnCCD layout.

- Thank you to Jeff Davis and Henning Ryll for proofreading this thesis.

- I would like to acknowledge all colleagues involved in the development and processing of the detectors I worked with.

- I would like to express my thanks to Dr. Heike Soltau for her support and all colleagues at PNSensor and PNDetector for the nice atmosphere during my work.

A special thanks to my family and friends, for their encouragement and support.